PROM PROGRAMMER
Program Card Set
909/919-1063-4

025-1063-4 REV S FEB 80

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TABLE OF CONTENTS

SECTION 1. SPECIFICATIONS

1.1 INTRODUCTION 1-1

1.2 CALIBRATION PROGRAM ADAPTER 1-1

1.3 CALIBRATION REQUIREMENTS 1-2

SECTION 2. INSTALLATION

2.1 DIGITAL CARD JUMPERS 2-1

2.2 CARD SET INSERTION 2-1
2.2.1 Models 1-5 2-1
2.2.2 Models 7 and 9 2-2
2.2.3 Systems 17 and 19 2-2

SECTION 3. OPERATION

SECTION 4. CALIBRATION

4.1 INTRODUCTION 4-1

4.2 TEST SET-UP 4-1
4.2.1 Models 1-5 4-1
4.2.2 Model 9 4-3
4.2.3 System 19 4-3

4.3 PROCEDURES FOR CALIBRATION 4-4
4.3.1 Check the State of the Start/Stop Line 4-5
4.3.2 Set the State of the Start/Stop Line 4-5
4.3.3 Set the State of the FWD/REV Line 4-5
4.3.4 Load Data onto the DI Bus 4-6
4.3.5 Confirm Data on the DO Bus 4-6

4.4 WAVEFORM OBSERVATION 4-7
4.4.1 Calibration Equipment Set-up 4-7
4.4.2 Test Procedure 4-7
4.4.3 Reject Jumper Reinstallation and Abort Test 4-9

SECTION 5. CIRCUIT DESCRIPTION

5.1 INTRODUCTION 5-1
5.1.1 Digital Card 5-1
5.1.2 Analog Card 5-1
5.1.3 Detailed Circuit Description 5-1

5.2 DIGITAL CARD 5-2
5.2.1 Select Gates 5-2
5.2.2 Program Memory 5-2
5.2.3 Clock Generator 5-2
5.2.4 Sequence Counter 5-2
5.2.5 Timing ROM 5-3
5.2.6 Overprogram Counter 5-3
5.2.7 Program pulse count and mode control 5-3
5.2.8 Bit Counter 5-3

5.2.9 Abort Timer 5-3
5.2.10 Pause Timer 5-3
5.2.11 Word Limit Select 5-3

5.3 ANALOG CARD 5-4
5.3.1 Bit Decoder 5-4
5.3.2 Program Voltage Generator 5-4
5.3.3 Vcc Generator 5-4
5.3.4 Comparators 5-5
5.3.5 VOL/VOH Buffer 5-5
5.3.6 DO Bus Drivers 5-5

SECTION 6. SCHEMATICS

LIST OF FIGURES

1-1 Parts included in the a)Programming Pak b)Program Card Set
2-1 Digital Card Jumper Locations
2-2 Installation of Card Set in Model 3 or 5
2-3 Installation of Card Set in Model 7 or 9
2-4 Installation of the Program Card Set in the Programming Pak
4-1 Set-up of Models 1-5 for DC Calibration
4-2 Set-up of Model 9 for DC Calibration
4-3 Set-up of System 19 for DC Calibration
4-4 Analog Card Adjustment Locations
4-5 Calibrator Set-up for the Waveform Observations
5-1 Simplified Block Diagram of Program Card Set
5-2 Block Diagram, 1225 Digital Card
5-3 Analog Card Block Diagram

LIST OF TABLES

1-1 Applications of the Program Card Set
2-1 Customer-Selectable Digital Card Jumpers

SECTION 1
SPECIFICATIONS

1.1 INTRODUCTION

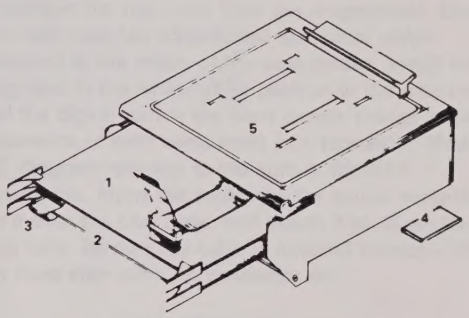
Data I/O Program Card Sets configure the programmer for the requirements of particular devices. This card set, used with the appropriate socket adapter, will program and read the devices listed in Table 1-1. New applications are developed frequently; therefore, consult the most recent Data I/O Comparison Chart of Programmable Devices to supplement Table 1-1.

Table 1-1. Applications of the Program Card Set

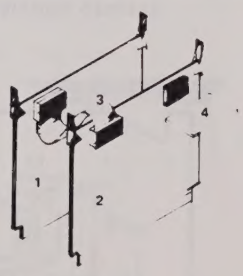
Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
HARRIS SEMICONDUCTOR				
32x8 FL	7602	VOL OC	16 PIN	1037
32x8 FL	7603	VOL TS	16 PIN	1037
256x4 FL	7610	VOL OC	16 PIN	1035-1
256x4 FL	7611	VOL TS	16 PIN	1035-1
512x4 FL	7620	VOL OC	16 PIN	1035-2
512x4 FL	7621	VOL TS	16 PIN	1035-2
512x8 FL	7640	VOL OC	24 PIN	1033-2
512x8 FL	7641	VOL TS	24 PIN	1033-2
512x8 FL	7646R	VOL OC	24 PIN	1411-2
512x8 FL	7647R	VOL TS	24 PIN	1411-2
512x8 FL	7648	VOL OC	20 PIN	1064
512x8 FL	7649	VOL TS	20 PIN	1064
1024x4 FL	7642	VOL OC	18 PIN	1039-3
1024x4 FL	7643	VOL TS	18 PIN	1039-3
1024x4 FL	7644	VOL OC	16 PIN	1042
1024x8 FL	7608	VOL TS	24 PIN	1033-3
1024x8 FL	7680	VOL OC	24 PIN	1033-3
1024x8 FL	7681	VOL TS	24 PIN	1033-3
2048x4 FL	7684	VOL OC	18 PIN	1039
2048x4 FL	7685	VOL TS	18 PIN	1039
2048x4 FL	7686	VOL OC	20 PIN	1394
2048x4 FL	7687	VOL TS	20 PIN	1394
2048x8 FL	76160	VOL OC	24 PIN	1033
2048x8 FL	76161	VOL TS	24 PIN	1033
MOTOROLA				
512x4 FL	7620	VOL OC	16 PIN	1035-2
512x4 FL	7621	VOL TS	16 PIN	1035-2
512x8 FL	7640	VOL OC	24 PIN	1033-2
512x8 FL	7641	VOL TS	24 PIN	1033-2
1024x4 FL	7642	VOL OC	18 PIN	1039-3
1024x4 FL	7643	VOL TS	18 PIN	1039-3
1024x8 FL	7680	VOL OC	24 PIN	1033-3
1024x8 FL	7681	VOL TS	24 PIN	1033-3
2048x4 FL	7684	VOL OC	18 PIN	1039
2048x4 FL	7685	VOL TS	18 PIN	1039

The Program Card Set includes the parts listed in Figure 1-1. The analog card produces the correct voltages in the proper waveforms for the device to be programmed or read. The digital card controls the sequences and shapes of these waveforms.

A Program Card Set for use in a System 17 or 19 Programmer is included in a Programming Pak and designated by a 919- part number. See Figure 1-1 a). A card set shipped alone, for use in a Model 1-5, 7 or 9 Programmer, bears a 909-part number. See Figure 1-1 b).



a) Programming Pak for System 17 and 19 Programmers



b) Program Card Set for Model 1-9 Programmers

1. DIGITAL CARD	701-1225
2. ANALOG CARD	701-1063-4
3. INTERCONNECT CABLE	701-1608
4. CALIB. PROGRAM ADAPTER	910-1063-4
5. PROGRAMMING PAK CARRIER	940-0919

Figure 1-1. Parts included in the a) Programming Pak b) Program Card Set

1.2 CALIBRATOR PROGRAM ADAPTER

The card set includes a Calibrator Program Adapter which mates with the Data I/O Universal Calibrator (P/N 910-1071). The PROMs on the adapter deliver the control signals to the analog card.

Using the calibrator and following the calibration procedure in Section 4 of this manual, Data I/O customers can be sure the Program Card Set remains within voltage and timing tolerances for effective programming.

1.3 CALIBRATION REQUIREMENTS

The need for calibration varies with the amount of use; calibration is recommended every ninety days of regular use or if programming yields fall below manufacturer's recommended minimums.

Complete calibration must be performed with a programmer that has an address and data display. Card sets for use in a Model 7 or System 17 may be properly calibrated using another Data I/O programmer. Alternately, Data I/O provides calibration service at regional Service Centers.

SECTION 2
INSTALLATION

2.1 DIGITAL CARD JUMPERS

Figure 2-1 shows the customer-selectable jumper locations on the digital card. Refer to Table 2-1 to check the jumper positions. If a jumper change is ever made, be sure to replace the jumpers in the normal position before using the card set for programming.

Table 2-1. Customer - Selectable Digital Card Jumpers

JUMPER	FUNCTION	NORMAL POSITION	COMMENTS
JP7	Reject	C	
JP10	Word Limit	2048	Selection defaults to socket adapter

2.2 CARD SET INSERTION

When changing card sets in Model 1-9 Programmers, turn power OFF.

Power may remain ON when changing Programming Paks in System 17 or 19 Programmers. In this way, data may be retained in RAM during the operation.

2.2.1 MODELS 1-5

Refer to Figure 2-2.

Remove the top cover from the programmer. Each card in the card cage has color-coded extractors which correspond to the colors of the card guides. Install the analog card in the white/white position in the card cage. Install the digital card in the front brown/orange position. Components of both cards must face forward in Model 3 and 5 Programmers and to the right in Model 1 Programmers. Insert the cable into the socket receptacle, route it over the card cage, and attach it to J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

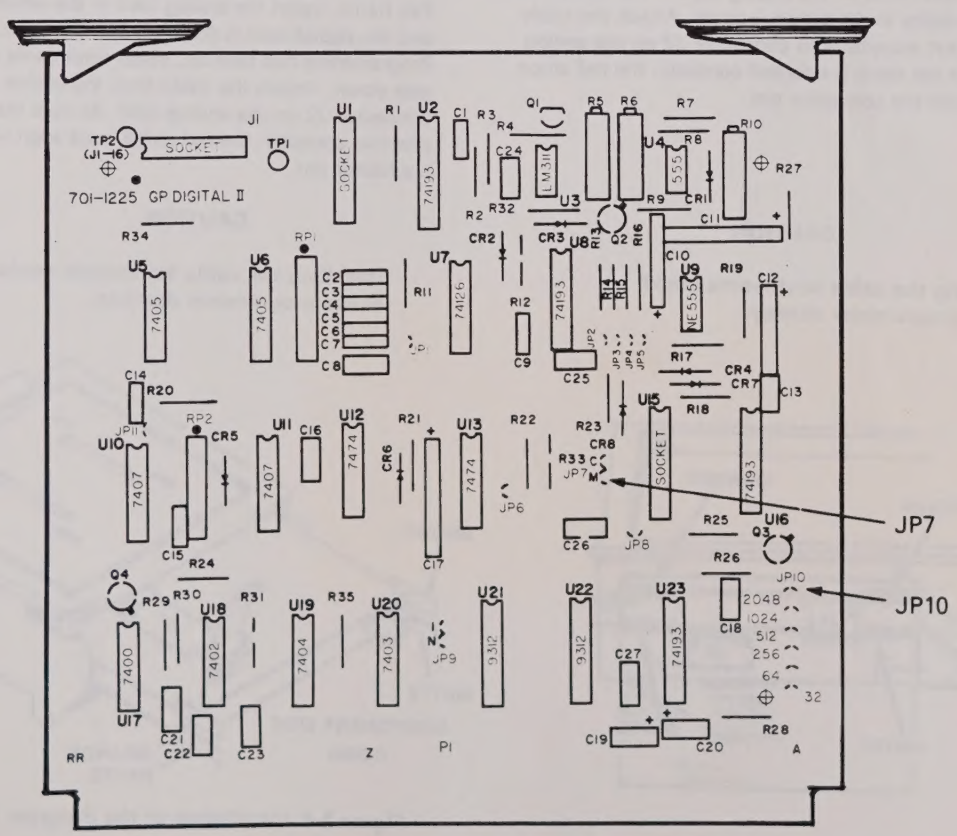


Figure 2-1. Digital Card Jumper Locations

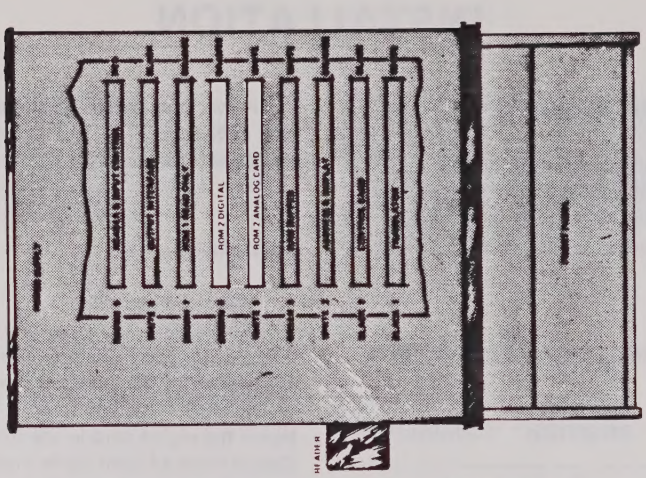


Figure 2-2. Installation of Card Set in Model 3 or 5

2.2.2 MODELS 7 AND 9

Refer to Figure 2-3.

The card set access door is located at the front of the programmer on the right-hand side. Open the door from the bottom to expose the card slots. The card guides are colored white/white and brown/orange to correspond with the extractor tabs on the cards. Insert both cards component-side-down — the analog card in the white/white slot and the digital in the brown/orange. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

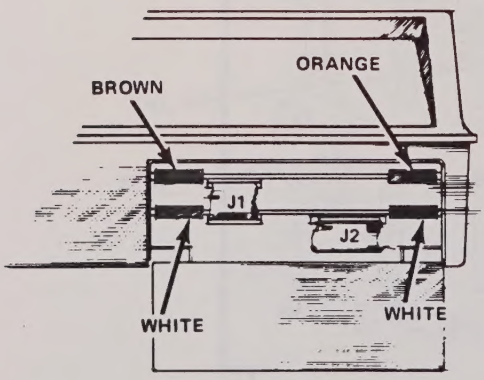


Figure 2-3. Installation of Card Set in Model 7 or 9

2.2.3 SYSTEMS 17 AND 19

Refer to Figure 2-4.

The card set should normally remain in the Programming Pak frame. Install the Programming Pak into the programmer by sliding it into the opening and lowering into position. Press gently on the handle to insure connector mating.

If the card set needs to be installed in its Programming Pak frame, insert the analog card in the white/white slot and the digital card in the brown/orange slot. With the Programming Pak face up, install both cards component-side-down. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

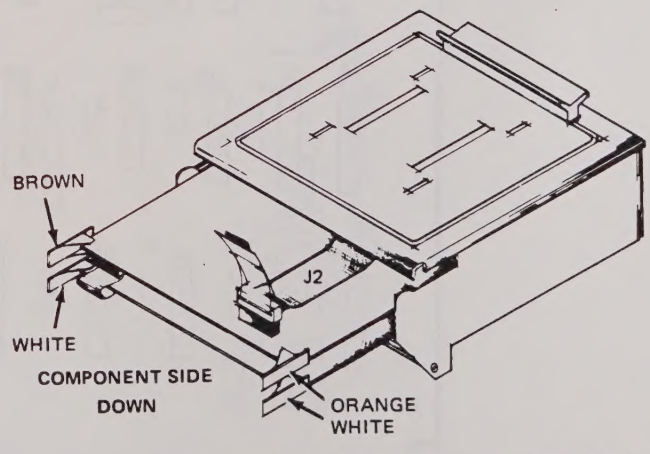


Figure 2-4. Installation of the Program Card Set in the Programming Pak

SECTION 3
OPERATION

The Program Card Set provides the link between the device in the socket adapter and the programmer's memory and control electronics. Its functions are directly controlled by the programmer. Complete instructions for operations using the card set are in the programmer instruction manual.

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Calibration Chart

DATA I/O
Programming systems for tomorrow...today

S ECN # 3431 2-[illegible]

CALIBRATION CHART 017-1063-4 PROGRAM CARD 909-1063-4

FIXTURE 702-1071 MANUFACTURER HARRIS

PAGE 1 OF 3 PROGRAM ADAPTER 910-1063-4 PROM HARRIS GENERIC FAMILY

DATE	REV	REVISION RECORD	DR	CK
12-77	P	ECN #1977	DS	RT
3-78	-	ECN #2122	RT	RT
6-78	R	ECN #2313	KJ	RT
7-28-78	S	ECN #2369	DB	SC
4-79		ECN #2565	FS	

COMMENTS
- Use paragraphs 4.3.1-4.3.5 for key sequences for COMMENTS below.
- **Switch S1 must be depressed for accurate readings.**
- CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U2	U1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	
00	10	+ 24	1-1	000	00	000			+24	R26	23.5	24.0	24.5	Adjustments located on power supply board.
00	10	POWER + 48	1-2	000	00	000			+48	R24	49.4	49.7	49.8	
00	10	SUPPLIES + 5	1-3	000	00	000			+ 5	R18	5.05	5.10	5.15	See programmer manual.
00	10	- 9	1-4	000	00	000			- 9	R40	-9.2	-9.0	-8.8	
00	10	PROGRAMMABLE SUPPLY	1-5	000	00	000			PROG V		15.5		17.5	
00	10	$\overline{CP}$ VIH	2-1	000	00	000	3	6	TP3		2.4		2.7	
00	00	$\overline{CP}$ VIL	2-2	001	01	001	10	6	TP3		0.0		0.4	
00	00	$\overline{CE2}$ VIH (2)	3-1	001	01	001	2	5	TP3		2.4		2.7	
00	09	$\overline{CE2}$ VIL	3-2	002	02	002	10	5	TP3		0.0		0.4	
00	09	COMPARATOR REFERENCE (FWD)	4-1	002	02	002	-	-	U5 P6		1.5		1.9	Test point located on analog card.
00	0D	COMPARATOR REFERENCE (REV)	4-2	003	03	003	-	-	U5 P6		0.8		1.1	Test point located on analog card.
00	0D	$\overline{VOL}$/VOH	5-1	003	03	003	3	7	TP3		2.4		2.7	
00	05	VCC READ	6-1	004	04	004	5	1	TP3	R46	4.8	5.0	5.2	*Adjustment Step.*
00	09	VCC VERIFY FWD	6-2	005	05	005	5	1	TP3	R47	5.2	5.5	5.7	*Adjustment Step.*
00	0D	VCC VERIFY REV	6-3	006	06	006	5	1	TP3	R45	4.3	4.5	4.7	*Adjustment Step.*
20	05	VCC PROGRAM (1)	6-4	007	07	007	5	1	TP3	R44	12.0	12.25	12.50	*Adjustment Step.*
20	05	ICC LIMIT	6-5	007	07	007	6	1	TP3		9.5		12.0	
00	01	VCC KILL	6-6	008	08	010	7	1	TP3		0.0		0.4	
20	E6	BIT 8 VOP	7-1	009	09	011	7	8	TP3		12.0		12.5	
20	E6	BIT 8 I LIMIT	7-2	009	09	011	5	8	TP3		2.0		2.8	
20	C6	BIT 8 DESELECT	7-3	010	0A	012	8	8	TP3		0.0		0.4	
20	C6	BIT 7 VOP	7-4	010	0A	012	7	9	TP3		12.0		12.5	
20	C6	BIT 7 I LIMIT	7-5	010	0A	012	5	9	TP3		2.0		2.8	
20	A6	BIT 7 DESELECT	7-6	011	0B	013	8	9	TP3		0.0		0.4	
20	A6	BIT 6 VOP	7-7	011	0B	013	7	10	TP3		12.0		12.5	
20	A6	BIT 6 I LIMIT	7-8	011	0B	013	5	10	TP3		2.0		2.8	
20	86	BIT 6 DESELECT	7-9	012	0C	014	8	10	TP3		0.0		0.4	
20	86	BIT 5 VOP	7-10	012	0C	014	7	11	TP3		12.0		12.5	
20	86	BIT 5 I LIMIT	7-11	012	0C	014	5	11	TP3		2.0		2.8	

CALIBRATION CHART 017-1063-4

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	
20	66	BIT 5 DESELECT	7-12	013	0D	015	8	11	TP3		0.0		0.4	
20	66	BIT 4 VOP	7-13	013	0D	015	7	12	TP3		12.0		12.5	
20	66	BIT 4 I LIMIT	7-14	013	0D	015	5	12	TP3		2.0		2.8	
20	46	BIT 4 DESELECT	7-15	014	0E	016	8	12	TP3		0.0		0.4	
20	46	BIT 3 VOP	7-16	014	0E	016	7	23	TP3		12.0		12.5	
20	46	BIT 3 I LIMIT	7-17	014	0E	016	5	23	TP3		2.0		2.8	
20	26	BIT 3 DESELECT	7-18	015	0F	017	8	23	TP3		0.0		0.4	
20	26	BIT 2 VOP (4)	7-19	015	0F	017	7	22	TP3		12.0		12.5	
20	26	BIT 2 I LIMIT	7-20	015	0F	017	5	22	TP3		2.0		2.8	
20	06	BIT 2 DESELECT	7-21	016	10	020	8	22	TP3		0.0		0.4	
20	06	BIT 1 VOP (3)	7-22	016	10	020	7	21	TP3		12.0		12.5	
20	06	BIT 1 I LIMIT	7-23	016	10	020	5	21	TP3		2.0		2.8	
20	26	BIT 1 DESELECT	7-24	017	11	021	8	21	TP3		0.0		0.4	
80	05	BIT 8 COMPARATOR	8-1	018	012	022	6	8						Confirm bit 8 ON (Hex 7F) on DO Bus.
80	05	BIT 7 COMPARATOR	8-2	018	012	022	6	9						Confirm bit 7 ON (Hex BF) on DO Bus.
80	05	BIT 6 COMPARATOR	8-3	018	012	022	6	10						Confirm bit 6 ON (Hex DF) on DO Bus.
80	05	BIT 5 COMPARATOR	8-4	018	012	022	6	11						Confirm bit 5 ON (Hex EF) on DO Bus.
80	05	BIT 4 COMPARATOR	8-5	018	012	022	6	12						Confirm bit 4 ON (Hex F7) on DO Bus.
80	05	BIT 3 COMPARATOR	8-6	018	012	022	6	23						Confirm bit 3 ON (Hex FB) on DO Bus.
80	05	BIT 2 COMPARATOR	8-7	018	012	022	6	22						Confirm bit 2 ON (Hex FD) on DO Bus.
80	05	BIT 1 COMPARATOR	8-8	018	012	022	6	21						Confirm bit 1 ON (Hex FE) on DO Bus.
20	C6	A0 VIL (5)	9-1	682	2AA	1252	3	20	TP3		0.0		0.4	
20	C6	A1 VIH	9-2	682	2AA	1252	3	19	TP3		2.4		2.7	
20	C6	A2 VIL	9-3	682	2AA	1252	3	18	TP3		0.0		0.4	
20	C6	A3 VIH	9-4	682	2AA	1252	3	17	TP3		2.4		2.7	
20	C6	A4 VIL	9-5	682	2AA	1252	3	16	TP3		0.0		0.4	
20	C6	A5 VIH	9-6	682	2AA	1252	3	15	TP3		2.4		2.7	
20	C6	A6 VIL	9-7	682	2AA	1252	3	14	TP3		0.0		0.4	
20	C6	A7 VIH	9-8	682	2AA	1252	3	13	TP3		2.4		2.7	
20	C6	A8 VIL	9-9	682	2AA	1252	3	2	TP3		0.0		0.4	
20	C6	A9 VIH	9-10	682	2AA	1252	3	3	TP3		2.4		2.7	

L. ADAPT. EX DATA DS. LOGIC) OCATION 2 U 1		TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT			SWITCH POSITIONS		MEASUREMENT					CALIBRATION CHART 017-1063-4 PAGE 3 OF 3
				DEC	HEX	OCT	S2	S3	TEST PT.	ADJ.	LIMITS MIN	LIMITS NOM	LIMITS MAX	
0	C6	A10 VIL	9-11	682	2AA	1252	3	4	TP3		0.0		0.4	
0	C6	A0 VIH	9-12	1365	555	2525	3	20	TP3		2.4		2.7	
0	C6	A1 VIL	9-13	1365	555	2525	3	19	TP3		0.0		0.4	
0	C6	A2 VIH	9-14	1365	555	2525	3	18	TP3		2.4		2.7	
0	C6	A3 VIL	9-15	1365	555	2525	3	17	TP3		0.0		0.4	
0	C6	A4 VIH	9-16	1365	555	2525	3	16	TP3		2.4		2.7	
0	C6	A5 VIL	9-17	1365	555	2525	3	15	TP3		0.0		0.4	
0	C6	A6 VIH	9-18	1365	555	2525	3	14	TP3		2.4		2.7	
0	C6	A7 VIL	9-19	1365	555	2525	3	13	TP3		0.0		0.4	
0	C6	A8 VIH	9-20	1365	555	2525	3	2	TP3		2.4		2.7	
0	C6	A9 VIL	9-21	1365	555	2525	3	3	TP3		0.0		0.4	
0	C6	A10 VIH	9-22	1365	555	2525	3	4	TP3		2.4		2.7	
0	C6	GROUND TEST	10-1	1365	555	2525	8	24	TP3		0.0		0.08	
20	C6	DATA PATTERN FOR ALL WORDS NOT SHOWN												

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Calibration includes checks of power supply levels, steady-state tests of critical programming parameters, and verification of resistively loaded programming waveforms. The need for calibration varies with the amount of use, but calibration is suggested at least every ninety days. For calibration by the customer, the procedure in this section should be followed in sequence.

NOTE

If any adjustment is necessary, complete the entire calibration procedure.

4.2 TEST SET-UP

The following equipment is required to perform a calibration:

a. Data I/O Universal Calibrator, P/N 910-1071

b. Calibration Extender:

Models 1-5	P/N 910-1136
Model 9	P/N 910-1074
System 19	P/N 910-1521

c. Digital voltmeter (DVM) — Fluke Model 8000A or equivalent.

d. A potentiometer adjustment tool

e. Dual-trace oscilloscope — Tektronix 465 or equivalent

f. A jumper wire approximately 12 inches in length

g. Data I/O interconnection cables:

Models 1-5	P/N 709-1613
Model 9	P/N 709-2608, 709-1613
System 19	P/N 709-2612, 709-1613

h. Calibrator Program Adapter

To prepare for calibration of the programmer power supplies and the Program Card Set, remove the card set from the programmer and connect the Universal Calibrator according to the following instructions:

4.2.1 MODELS 1-5

Refer to Figure 4-1.

a. Make sure the programmer power is OFF.

b. Remove the cover from the programmer and remove the Program Card Set from the card cage.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

d. Install the Extender Card, P/N 910-1136, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card in the digital card position (brown/orange) in the programmer card cage.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

RESET
ROM2 — ROM2
MANUAL
PROGRAM
START

Figure 4-1. Set-up of Models 1-5 for DC Calibration.

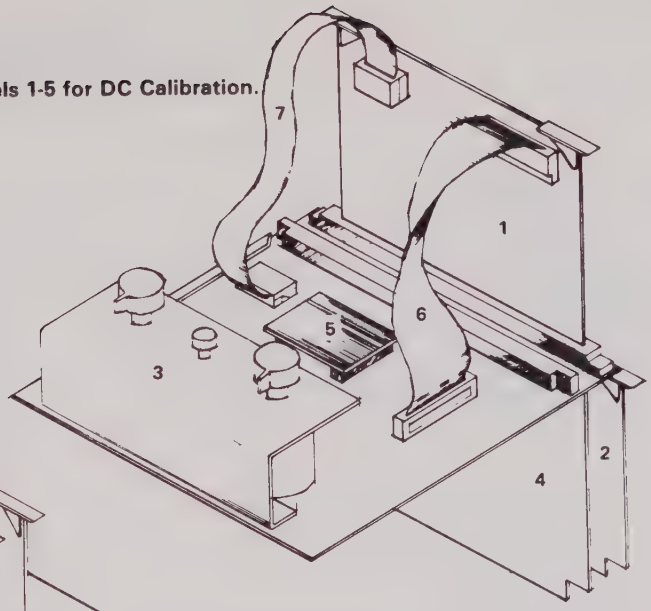
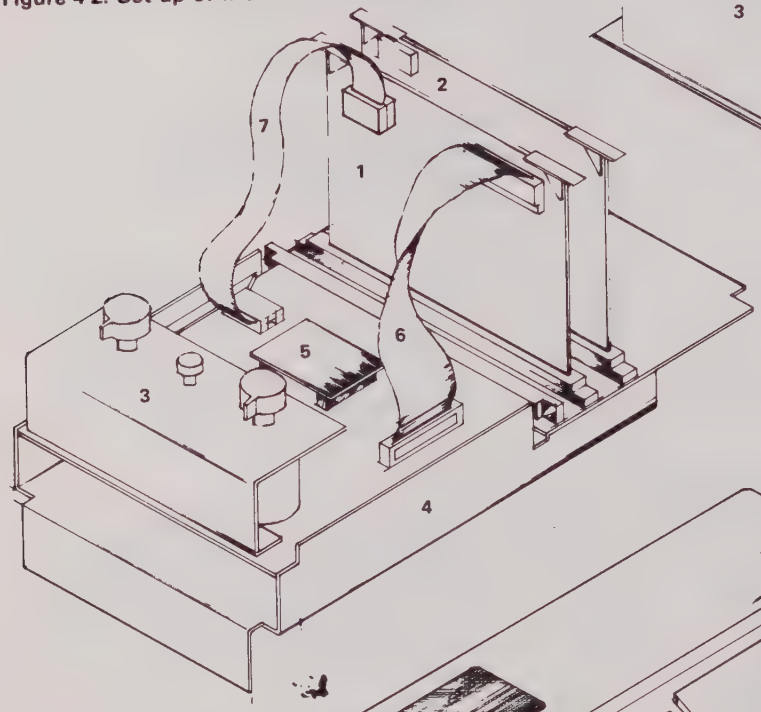
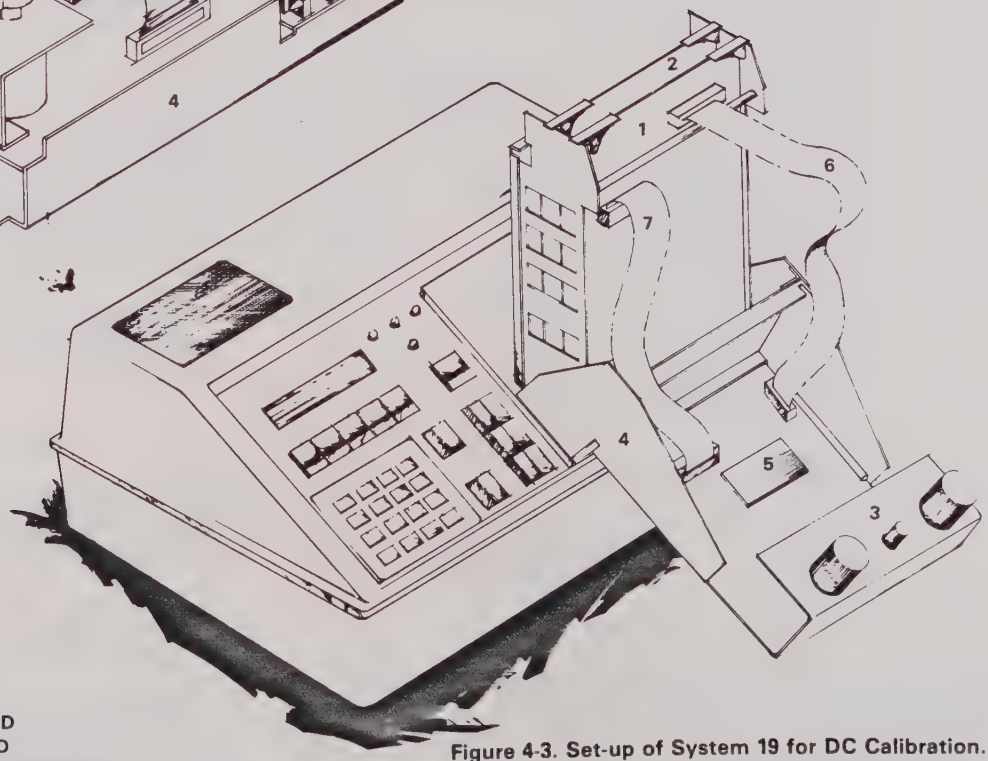


Figure 4-2. Set-up of Model 9 for DC Calibration.





1. ANALOG CARD
2. DIGITAL CARD
3. UNIVERSAL CALIBRATOR
4. CALIBRATION EXTENDER
5. CALIBRATOR PROGRAM ADAPTER
6. 26-CONDUCTOR CABLE
7. 16-CONDUCTOR CABLE

Figure 4-3. Set-up of System 19 for DC Calibration.

4.2.2 MODEL 9

Refer to Figure 4-2.

a. Make sure the programmer power is OFF.

b. Open the Program Card Set access door from the bottom. Remove the Program Card Set.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

d. Install the Extender Card, P/N 910-1074, (with the Universal Calibrator attached) into the programmer's digital card position (brown/orange). Be sure that the edge of the Extender Card is securely seated. Install the Digital and Analog cards into the 1074 calibration extender according to Figure 4-2.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

KEYBOARD
EXECUTE
NORMAL/INVERT switch to INVERT

4.2.3 SYSTEM 19

Refer to Figure 4-3.

a. Make sure the programmer power is OFF.

b. Remove the Programming Pak from the programmer.

c. Insert the Calibration Extender, P/N 910-1521, in the same way as the Programming Pak, being sure to seat it properly in the programmer's mating connector.

d. With the handle of the Programming Pak down, connect the 64-pin connectors of the Programming Pak and Calibration Extender. Be sure the connectors mate securely.

e. Slide the Universal Calibrator securely into the card slots at the front of the Calibration Extender.

f. Connect the 26-conductor cable from J2 of the analog card to J2 of the Universal Calibrator, making sure to align the red stripe with the connector dot.

g. Disconnect the 16-conductor cable from J1 on the digital card and route it to J1 on the Universal Calibrator, making sure to align the red stripe with the connector dot.

h. Plug the Calibrator Program Adapter into the Program Adapter slot on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number of the Calibrator Program Adapter corresponds to the 919-XXXX part number of the Programming Pak.

i. Connect the DVM ground lead to GND test point on the Universal Calibrator.

j. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

SELECT
C1 (calibrate ON)
START

k. Press:

KEYBD
ENTER

The TEST light comes ON and remains ON throughout calibration.

NOTE
To exit calibration, press:
SELECT
C0 (calibrate OFF)
START
(Test light goes OFF.)

l. Press START.

4.3 PROCEDURES FOR CALIBRATION

The Calibration Chart, between pages 4-4 and 4-5, gives the steps for complete DC calibration. It is to be used only with the Calibrator Program Adapter specified in the title block of the chart.

The first five steps on the Calibration Chart cover the level checks of the programmer power supplies. If any adjustment is necessary in these steps, refer to the Programmer Manual. The remaining steps provide information for calibration of the Program Card Set.

- The PROGRAMMER WORD COUNT column is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When performing each step, set the address (word count) corresponding to the address number base of the programmer in use. For instance, with a programmer having a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static conditions created by the Universal Calibrator may cause thermal damage to components if the programmer is left unattended with advanced word count.

- The TEST DESCRIPTION column specifies the function to be checked in each step. In most cases, the steps simply require a DVM reading to insure that a level is within tolerance. Some steps, labeled Adjustment Steps, give a nominal (NOM) value and prescribe adjustment to that value if the level is out of the MIN-MAX range.

- The ADJUSTMENT column calls out potentiometer designations. The first four entries in the ADJ column refer to power supply potentiometers located on the power supply board of the programmer. The remaining entries in the ADJ column refer to potentiometers on the analog card. Refer to Figure 4-4 for locations of the potentiometers.

- The SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load-select switch; S3 is the line-select switch. Each step on the Calibration Chart may require changing of switch positions. With the proper S2 and S3 positions selected, press S1 to make an accurate reading, and keep the switch depressed only long enough to complete the step.

CAUTION

DO NOT keep S1 depressed for extended periods. Certain measurements induce high programmer current levels. Extended high-current operation (S1 depressed) may damage sensitive electronic components.

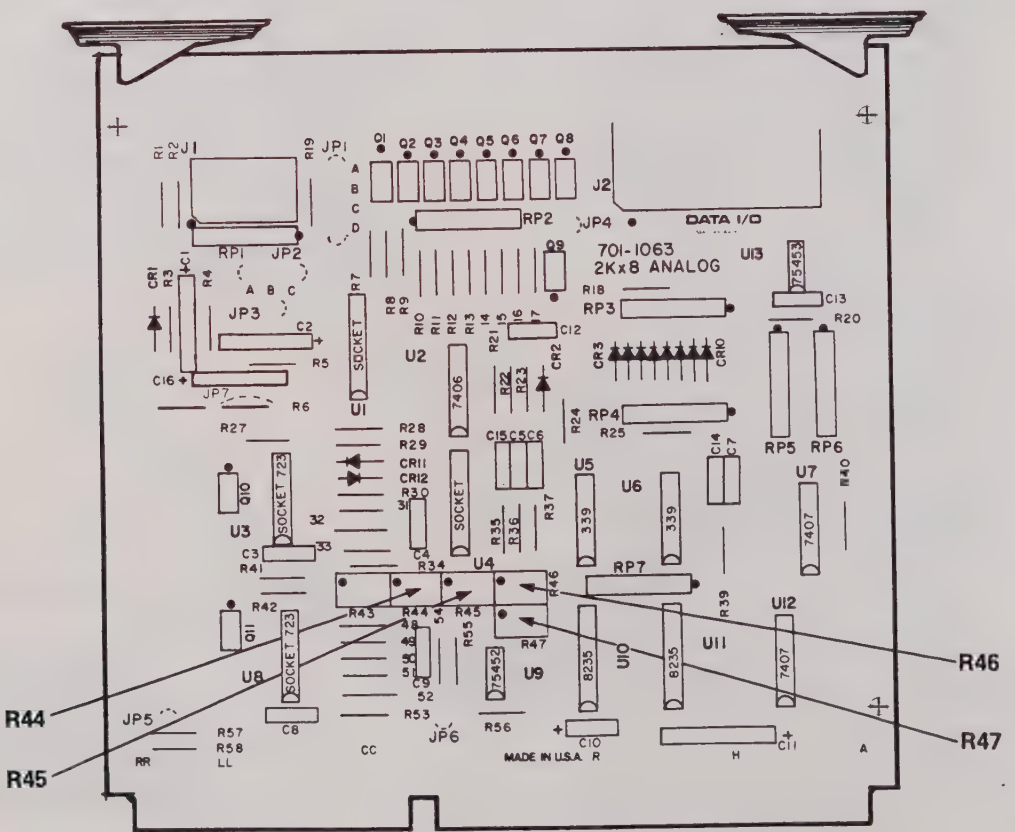


Figure 4-4. Analog Card Adjustment Locations

- The TEST POINT column gives test point locations for the DVM probe. Most test points are located on the Universal Calibrator; some points are located on the program card. For instance, if a test point is designated as U6 P8, the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the COMMENTS column.

- The LIMITS column is divided into three portions: MIN (minimum), NOM (nominal), and MAX (maximum). The values given are in volts and indicate the range into which a given DVM reading should fall. If a reading is within the limits, no adjustment is required and the programmer (or Program Card Set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (in adjustment steps), the card is nonfunctional and should not be used for programming.

- The COMMENTS column on the right side of the chart provides information for certain calibration steps including call-outs of programmer operations required in some steps. The programmer provides signals to the card set on the Address bus, the Data Input bus, the START/STOP line and the FWD/REV line. The card set provides signals to the programmer on the RESET line, the VOL/VOH select line and the Data Output bus. In the course of calibration, the programmer is used to observe or set the following conditions:

- State of the START/STOP line
- State of the FWD/REV line
- Data on the DO bus
- Data on the DI bus

Key sequences for observing these conditions are given in the following paragraphs (4.3.1 — 4.3.5). Follow the tests on the Calibration Chart step-by-step, and refer to paragraphs 4.3.1 — 4.3.5 as necessary.

MODEL 9 USERS NOTE

Some of the following operations are performed differently on Model 9's with different revisions of software. Perform the following test to determine whether to refer to steps for Revision "A" software or to steps for Revision "B" or later software.

1. *Turn power OFF.*
2. *Observe the LOAD indicator while turning power ON.*
3. *If the LOAD indicator remains ON, refer to key sequences for Revision "B" or later software.*
4. *If the LOAD indicator turns OFF, refer to key sequences for Revision "A" software.*

4.3.1 CHECK THE STATE OF THE START/STOP LINE

For steps that require confirmation of the state of the START/STOP line, perform the check as follows. To continue testing after confirming a STOP condition, START the programmer according to paragraph 4.3.2.

Models 1, 2, 3 and 5:	Observe the START and STOP indicators.
Model 9:	Press the PROM key and observe the data display. The programmer is in STOP if the display is blank; in START if the display shows data.
System 19:	Observe the START light. If the START light is on, the programmer is in START.

4.3.2 SET THE STATE OF THE START/STOP LINE

Models 1, 2, 3 and 5:	Press the START/STOP key.
Model 9:	a. Press KEYBOARD to stop. b. Press EXECUTE to start.
System 19:	a. To set the programmer in START, press KEYBD, ENTER and START. b. To set programmer in STOP, press KEYBD.

4.3.3 SET THE STATE OF THE FWD/REV LINE

To set the programmer in FORWARD or in REVERSE:

Models 1, 2, 3 and 5:	Press the FWD key or the REV key.
Model 9:	See MODEL 9 USERS NOTE, paragraph 4.3, to determine the right revision letter.
Revision "A" Software:	Halt the programmer in FWD and in REV by entering data at an address and causing a mis-verify: a. Ground J1-16 on the analog card. b. Press LOAD. c. Press EXECUTE. d. Press KEYBOARD. e. Key in data — Ø hex — at address ØØ1. f. Press VERIFY. g. Press EXECUTE. The programmer will mis-verify

at the address containing data and will STOP in FWD.

h. Press SKIP. The programmer will mis-verify at the address containing data and will halt in REV.

Revision "B" or later Software:

Press the FWD key to set the programmer in FORWARD and the REV key to set it in REVERSE.

System 19:

With KEYBD selected, press ENTER to set the programmer in FORWARD. Press ENTER and then REVIEW to set it in REVERSE.

4.3.4 LOAD DATA ONTO THE DI BUS

The data on the Calibration Chart is to be loaded on the DI bus using the programmer keyboard.

Models 1, 2 and 5:

Key in binary data called out on the Calibration Chart. (Bits called out must be ON, bits not called out must be OFF.) Perform the necessary number-system conversions if using an octal or hexadecimal keyboard. Confirm correct data by checking the binary DI display.

Model 3:

Use an external source, such as a paper tape reader, to put binary data on the DI bus.

Model 9:

(See MODEL 9 USERS NOTE, paragraph 4.3, to determine the correct revision letter.) When using a Model 9, always key in the hex data in parentheses to be sure that the correct data is placed on the DI bus.

Revision "A" Software

Halt the programmer in the automatic program mode with data on the DI bus.

a. Clear RAM: Select INVERT. Then press and hold the EDIT key while pressing LOAD.

b. Press the KEYBOARD key, and key in hex data called out in parentheses on the Calibration Chart.

c. Press the PROGRAM key.

d. Ground J1-16 on the analog card.

e. Press EXECUTE and wait for the programmer to abort.

f. Press STOP, KEYBOARD and EXECUTE.

g. Disconnect J1-16 from ground.

h. SET the address specified on the Calibration Chart in order to make the measurement.

Revision "B" or later Software:

With the KEYBOARD indicator illuminated and all the others OFF, use the hex keypad to key in hex data called out in parentheses on the Calibration Chart.

System 19:

a. Press KEYBD, key in the address and press ENTER.

b. Key the hex data in parentheses into RAM at the specified address.

c. Press ENTER and then REVIEW.

4.3.5 CONFIRM DATA ON THE DO BUS

Models 1, 2, 3 and 5:

Compare the bit callout on the Calibration Chart with the OUTPUT DATA display on the programmer front panel. Bits not called out must be OFF. Ignore the hex data on the chart.

Model 9:

With the EXECUTE light ON, press the PROM key and observe the data display on the programmer front panel. Data must match the hex callouts on the Calibration Chart.

System 19:

With KEYBD selected, press the DEVICE DATA key. Hold it down while reading the hex data. The programmer must be in START.

4.4 WAVEFORM OBSERVATION

Programming waveforms should be observed after complete DC calibration of the programmer and Program Card Set. Set-up instructions assume that the calibration equipment is already installed for calibration per paragraph 4.2.

In waveform observation, oscilloscope displays are to be compared with the Timing Diagram. These waveforms, indicated by circled digits on the Timing Diagram, have the same reference on the Calibration Chart. Waveforms are selected using Universal Calibrator switches S2 and S3 as specified on the Calibration Chart.

4.4.1 CALIBRATION EQUIPMENT SET-UP

Refer to Figure 4-5.

a. Make sure that the programmer power is OFF.

b. Remove the digital card from the card slot.

c. Check the Timing Diagram to determine the number of the reject jumper. Find and remove the jumper on the digital card (if installed), making sure to note the position in which it is installed.

CAUTION

Be sure to replace the reject (abort) jumper (if it was installed) in the proper position after waveform observation.

d. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

e. Connect the free end of the 16-conductor cable to digital card J1, making sure that the red cable stripe and pin 1 are properly oriented.

f. Connect the triggered input of a dual-trace oscilloscope to the digital-card test point as indicated to the left of the TEST waveform on the Timing Diagram. Connect an input probe to TP3 on the calibrator.

g. Reinstall the digital card in the slot from which it was removed.

h. Check the NOTES column on the Timing Diagram to determine whether the Program Card Set defaults to VOH or VOL for calibration. If and only if the card set defaults to VOH, ground J1-16 (Read Enable line) to the GND test point on the Universal Calibrator.

CAUTION

Do not connect J1-16 to any other potential; damage to programmer components may result.

4.4.2 TEST PROCEDURE

Observing programming waveforms requires putting data in RAM and causing the programmer to attempt to program a nonexistent device.

1. Turn programmer power ON.

2. Prepare the programmer for keyboard data entry.

Models 1—5, press:	RESET RAM-RAM PROGRAM MANUAL START
Model 9:	Set the NORMAL/INVERT switch in NORMAL if the Program Card Set is calibrated VOH or in the INVERT position if VOL. The NOTES column on the Timing Diagram specifies the correct polarity. Press: KEYBOARD.
System 19 press:	KEYBD Ø ENTER

3. Key in data for bit 1 at several addresses:

Models 1—5:	Enter bit 1 at several addresses and confirm that bit 1 is ON and all other bits are OFF on the DI display.
Model 9:	Enter hex data "Ø1" at several addresses.
System 19:	Enter hex data "Ø1" at several addresses. Check the NOTES column on the Timing Diagram to determine the correct data polarity. If the Timing Diagram indicates VOL, enter a hex "E" for 4-bit card sets; "FE" for 8-bit card sets.

4. Select the PROGRAM mode:

Models 1—5, press:	RESET PROGRAM AUTO RAM-ROM2

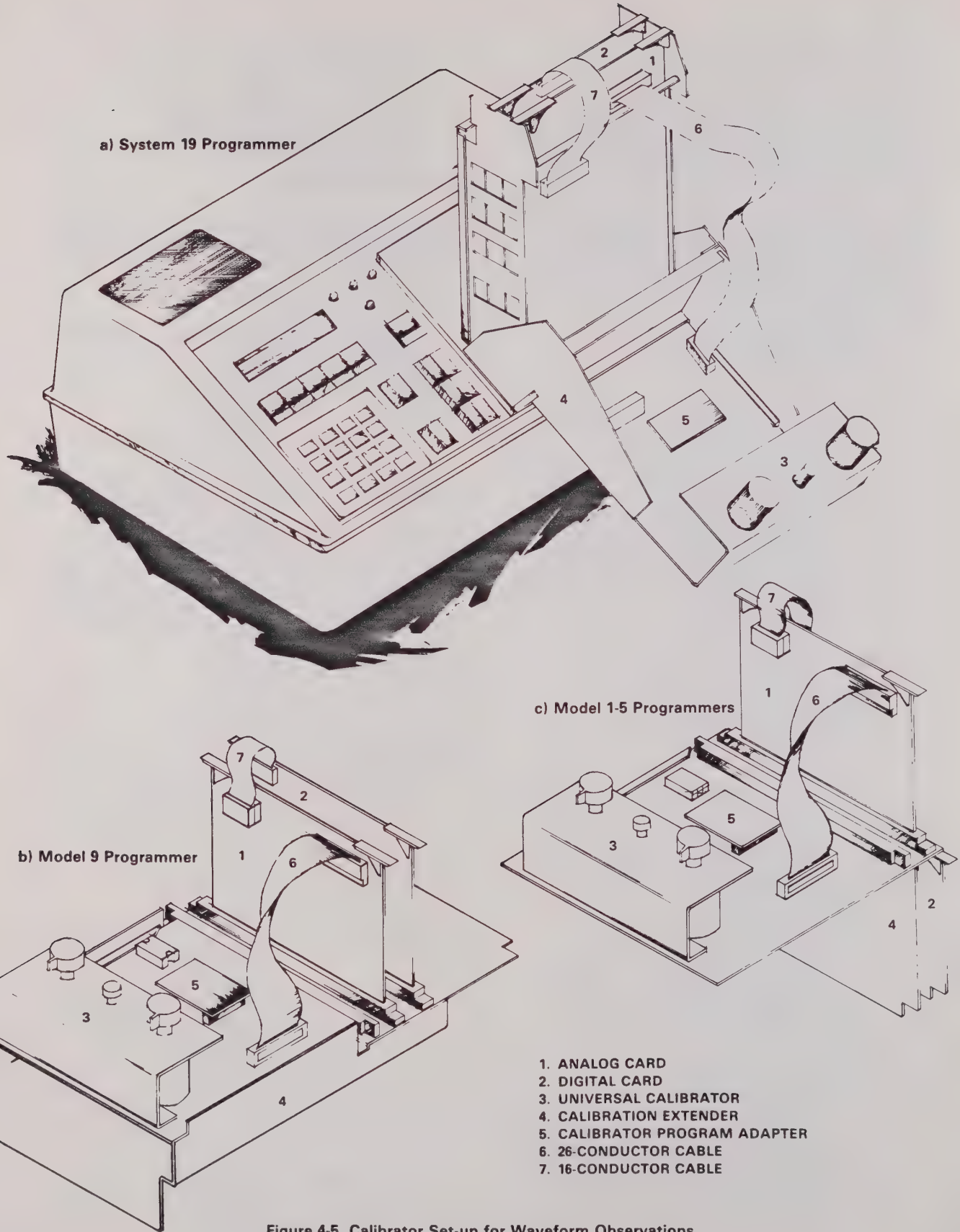


Figure 4-5. Calibrator Set-up for Waveform Observations

Model 9, press:	PROGRAM
System 19, press:	SELECT C1 START PROG

5. Initiate waveforms:

Models 1—5, press:	START
Model 9, press:	EXECUTE
System 19, press:	START

After initiating the programming sequence, the programmer will halt at the first address which has data. Refer to the Timing Diagram and Calibration Chart by the circled digits (1 , 2 , 3 , ...). Make the indicated switch selections with S2 and S3 on the Universal Calibrator.

Observe specific waveforms relative to the triggered test pulse by pressing S1 on the calibrator. S3 is used to route analog card output to TP3 (the oscilloscope probe); S2 selects resistive loads that are applied when S1 is pressed. All other information on the Calibration Chart is of no importance during waveform observation.

CAUTION

When S1 is depressed, high currents are induced within the programmer; do not hold S1 depressed for extended periods.

6. Stop programming:

Models 1—5 and 9, press:	STOP
System 19, press	KEYBD

4.4.3 REJECT JUMPER REINSTALLATION AND ABORT TEST

Before putting the Program Card Set back in use, it is necessary to reinstall the reject (abort) jumper and confirm the operation of the abort function on the digital card.

CAUTION

The reject jumper must be reinstalled. Otherwise, the programmer and/or cardset may be damaged by a prolonged attempt to program a defective device.

1. Turn the programmer power OFF.
2. Remove the digital card from the card slot.
3. Refer to the Timing Diagram for the reject jumper number and make sure to install the jumper in the position from which it was removed.
4. Reinstall the digital card in the card slot.
5. Repeat the key sequence in Waveform Test Procedure, paragraph 4.4.2, steps 1—5.
6. With Universal Calibrator switch positions selected to observe the test pulse waveform, repeat step 6 of the Test Procedure. Note with the oscilloscope that the waveform display is terminated by the programmer. This indicates that the abort function of the digital card is operative.

NOTE

The digital card has one or more potentiometers for calibrating various timing functions of the card set. In normal usage, the card set will rarely need to have these functions re-calibrated.

However, in the event that the card set waveforms do not conform to the specifications of the Timing Diagram, contact your nearest Data I/O Service Representative for calibration information.

SECTION 5
CIRCUIT DESCRIPTION

5.1 INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 5-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

5.1.1 DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses from the analog card until either ABORT or REJECT is signalled or until the bit is programmed.

5.1.2 ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturers' specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

5.1.3 DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow, timing and reject conditions. Detailed circuit schematics are found at the rear of this manual — refer to these for pin-out and interconnection information.

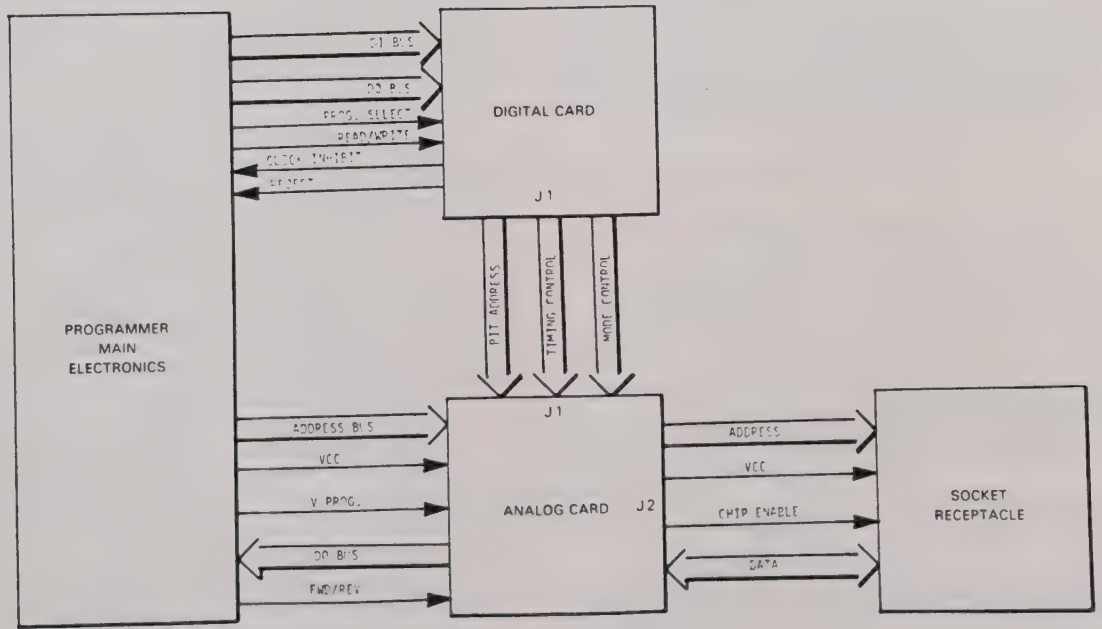


Figure 5-1. Simplified Block Diagram of Program Card Set

5.2 DIGITAL CARD

Figure 5-2 gives a generalized block diagram of the digital card. This diagram shows signal flow and functional relationships between the blocks but does not include detailed interconnect information. Refer to the schematics and timing diagram (with truth tables) for details of circuit connection and operation. The following paragraphs discuss the functions performed by the digital card.

5.2.1 SELECT GATES

U17 and U18 (on schematic) monitor Program Select (LL), Write Inhibit (PP), Read (X), and Read Inhibit (RR) in order to enable operation of the digital card. Output from Read Gate U17 is routed to the analog card to control the Data Bus Drivers. The Write Output Enable Gate allows the program Memory to be set.

5.2.2 PROGRAM MEMORY

When the digital card is selected for operation, the Program Memory will set upon receiving a Write command on AA. This causes the Clock Generator on the digital card to begin operation and halts the programmer. Initialization of the Program Pulse Counter, Bit Counter and Sequence Counter and clearing of the Overprogram Counter occur before the Program Memory is set.

5.2.3 CLOCK GENERATOR

When the Program Memory sets in response to the Write and Program Select commands, the Clock Generator begins operation and the programmer is inhibited. Clock pulses increment the Sequence Generator. Alternate clock rates are determined by the Mode ROM or by the High Order (H/O) Memory (with JP8 connected). The Clock may be halted by the Abort Timer or by the Pause Timer (with CR2 connected).

5.2.4 SEQUENCE COUNTER

The 4-bit Sequence Counter drives the 32x8 Timing ROM. The combination generates timing signals for analog control, along with Bit Test and Bit Increment pulses, which are used on the digital card. (See the Timing Diagram.) A clock pulse is also output for PROMs with registers.

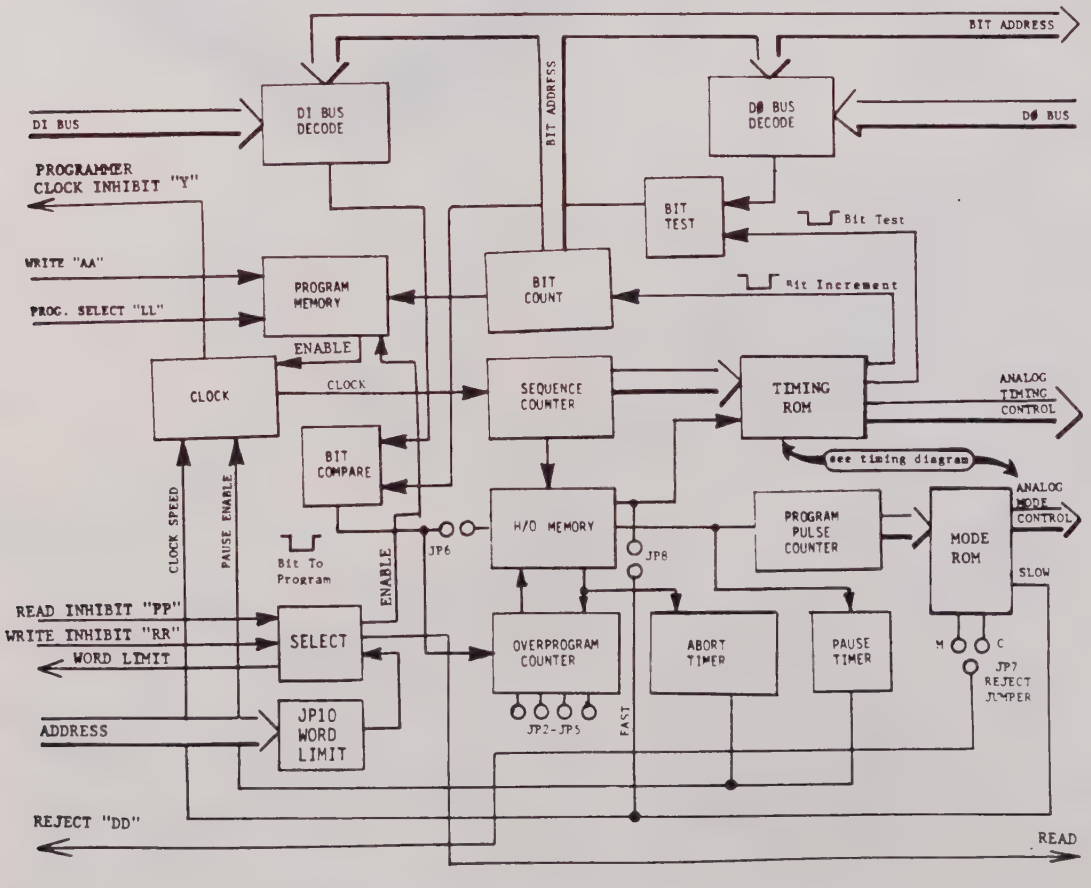


Figure 5-2. Block Diagram, 1225 Digital Card

5.2.5 TIMING ROM

Output words from the Timing ROM are used in the serial Verify and Program operations, as shown in the Timing Diagram. Verify operations use Low Order words 0 to 15; Program operations use High Order words 16 through 31. Words 8 through 11 are used to output control signals for Vcc voltages during Read and Verify operations, which occur under machine control when the digital card is not selected. Those words are loaded through the Sequence Counter to the Timing ROM, as determined by the FWD line and Write Inhibit. (See the Schematic.)

At the beginning of a programming sequence (word 2), the Timing ROM outputs a Bit Test pulse to the Bit Test gate. If the DO Bus Decoder determines that there is no bit already programmed in the PROM, and if the DI Bus Decoder determines that there is a bit to program, then the Compare Gate outputs a Bit to Program pulse.

5.2.6 OVERPROGRAM COUNTER

The Bit to Program pulse loads the Overprogram Counter and also sets the Bit to Program Memory. This, in turn, allows a carry pulse from the Sequence Counter to reach the high order memory. It also disables the Bit Count Gate until the Overprogram Counter clocks the Bit to Program Memory after the bit has been programmed.

At Timing ROM word 15, the carry pulse from the Sequence Counter toggles the H/O memory. This enables the fifth address line to the Timing ROM, and it advances into High Order (Program) Count, words 16 through 31.

At word count 31, the Sequence Counter outputs another carry pulse to again toggle the H/O memory. This sets the Timing ROM back to Low Order Count (Verify). At word 2, again, a Bit Test pulse is output from the Timing ROM; if the buses compare at Bit Test (bit is programmed), the output of the Bit Compare Gate remains unchanged (no Bit to Program), the H/O Memory remains enabled, and the Bit Count Gate remains disabled.

At word 15 the Sequence Counter outputs another carry pulse which again causes a High Order (Program) count, causing the Overprogram Counter to decrement. The above cycle repeats until the Overprogram Counter outputs a borrow pulse after counting down from the level preset by JP2—JP5. The borrow pulse resets the Bit to Program Memory which enables the Bit Count Gate, allowing it to decrement the bit count to the next bit.

Some 1225 cards are wired with JP6 shorted. With JP6 shorted, a Bit to Program pulse sets the High Order Memory. This causes the fifth address input line to the Timing ROM to go high, enabling the programming sequence of the Timing ROM. At word 31, the carry pulse from the Sequence Counter shifts the count sequence back to Low Order. With JP6 shorted, the total sequence is 16 pulses long.

5.2.7 PROGRAM PULSE COUNT AND MODE CONTROL

As program pulses are delivered to the PROM being programmed, the Program Pulse Counter counts up; outputs from the Program Pulse Counter are used as address line inputs to the Mode Control ROM. The Timing Diagram includes the truth table for the Mode Control ROM. Outputs of the Mode ROM control the magnitude of the program pulses (bits 1 and 2), along with clock speed (bit 3). Bits 4 and 5 control the number of programming attempts allowed before a reject is signalled to the programmer; reject jumper JP7 selects either the M line or the C line. (See the Timing Diagram for the pulse numbers selected.)

5.2.8 BIT COUNTER

The Bit Counter counts bit increment pulses arriving from the Timing ROM through the Bit Counter Gate. This gate is disabled, halting the Bit Counter, when the Bit to Program Memory is set by a Bit-to-Program pulse. The Bit Counter counts down from either 4 or 8, as determined by the socket adapter or the Mode ROM. Output from the Bit Counter controls the DO Bus Decoder and DI Bus Decoder as well as the Bit Decoder on the Analog Card. When the Bit Counter reaches zero, its borrow output is used to reset the Program Memory.

5.2.9 ABORT TIMER

The Abort Timer measures the time required to program a bit. If programming time is excessive, and JP1 is shorted, a REJECT is signaled and the clock is halted. The Abort Timer is connected to the Overprogram Counter such that an abort is possible only during Low Order Count (Verify cycle). Some card sets don't use this function.

5.2.10 PAUSE TIMER

Some card sets use the Pause Timer to measure the time to program the PROM. A transistor is used in conjunction with the timing components to integrate out the time that the Program Memory is set. If programming time exceeds the value set by circuit components, the Clock is stopped in order to allow the PROM to cool; after a pause in the order of seconds the Clock is allowed to start again, and programming continues. The Pause Timer output is gated with the Timing ROM so that a pause cannot occur during program pulses.

5.2.11 WORD LIMIT SELECT

Word Limit is jumper-selected at JP10 on the digital card to 32, 64, 256, 512, 1024, or 2048. JP10 limits the address range of the programmer through the Word Limit line (CC), according to the configuration of the PROM being programmed. Selection defaults to the socket adapter.

5.3 ANALOG CARD

The analog card receives control signals from the digital card via J1 and from the programmer via edge contacts. Figure 5-3 shows signal flow from analog card components to the PROM being programmed. Refer to the truth tables on the Timing Diagram for precise details about signal amplitudes and timing.

5.3.1 BIT DECODER

PROM bits are programmed individually within a given PROM word. Bit information arrives at analog card J1 and is used to drive the Bit Decoder, U1. Decoder outputs enable the appropriate Bit Program Switches and transfer program pulses to the bit lines of the PROM being programmed.

During the appropriate clock periods of the Program cycle (see the Timing Diagram) the bit switches are turned ON. On 1063-2 and 1063-5 cards, these switches connect the output of the Program Voltage Generator to the PROM bit lines. On 1063-3 and 1063-4 cards, the bit switches ground the PROM bit lines. The Program Voltage Generator is not used on those cards. Instead, programming current is provided by the Vcc Generator.

5.3.2 PROGRAM VOLTAGE GENERATOR

The Program Voltage Generator (1063-2 and 1063-5 only) is a current limited IC regulator. It supplies current for burning the PROM bits.

5.3.3 Vcc GENERATOR

The Vcc Generator is a current-limited regulator with five selectable states: Vcc Kill, Vcc Program, Vcc Verify Forward, Vcc Verify Reverse, and Vcc Read.

On 1063-3 cards, Vcc Kill is used during the programming sequence to reduce the average power dissipation and improve programming yield. It also is used on 1063-5 cards in STOP, to remove Vcc from the PROM socket during insertion and removal of the PROM.

Vcc Program is selected while programming pulses are actually being applied to the PROM. After the programmer completes the forward and reverse programming passes, it enters the Verify mode. Vcc Vfy Fwd and Vcc Vfy Rev are used for parametric verification during the forward and reverse passes in the Verify mode. These levels are also used during the reading of the PROM when it is selected as an output device.

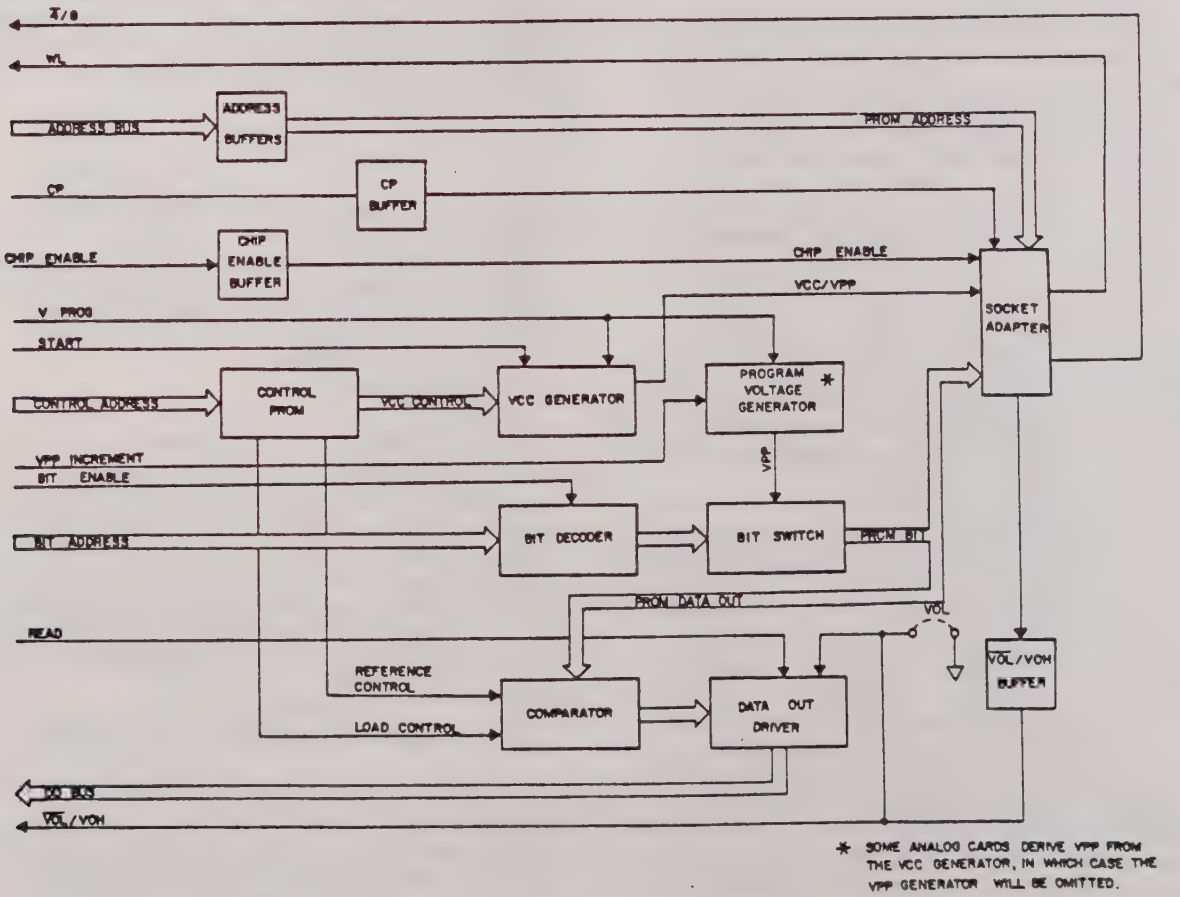


Figure 5-3. Analog Card Block Diagram

V_{CC} Read is used during the reading of the PROM when it is selected as an input device. This level is also used during the Read portion of the programming cycle.

These levels are all selected via the Control ROM, U4, by signals from the digital card, and with the exception of V_{CC} Kill they are adjustable by potentiometers R44-R47. Refer to the Timing Diagram for these voltage levels, and refer to the Calibration section for adjustment information.

5.3.4 COMPARATORS

The Comparators read the data at the output of the PROM under selectable load and threshold conditions.

The two thresholds are derived from voltage dividers under the control of ROM U4, and establish read thresholds for Read, Program, and Verify operations.

The load switch (depending on the number of the card set) provides the manufacturer's specified load during Read, isolation during Program for bits not being programmed, and/or the specified parametric load during Verify. The load also is controlled via U4 by signals from the digital card.

5.3.5 VOL/VOH BUFFER

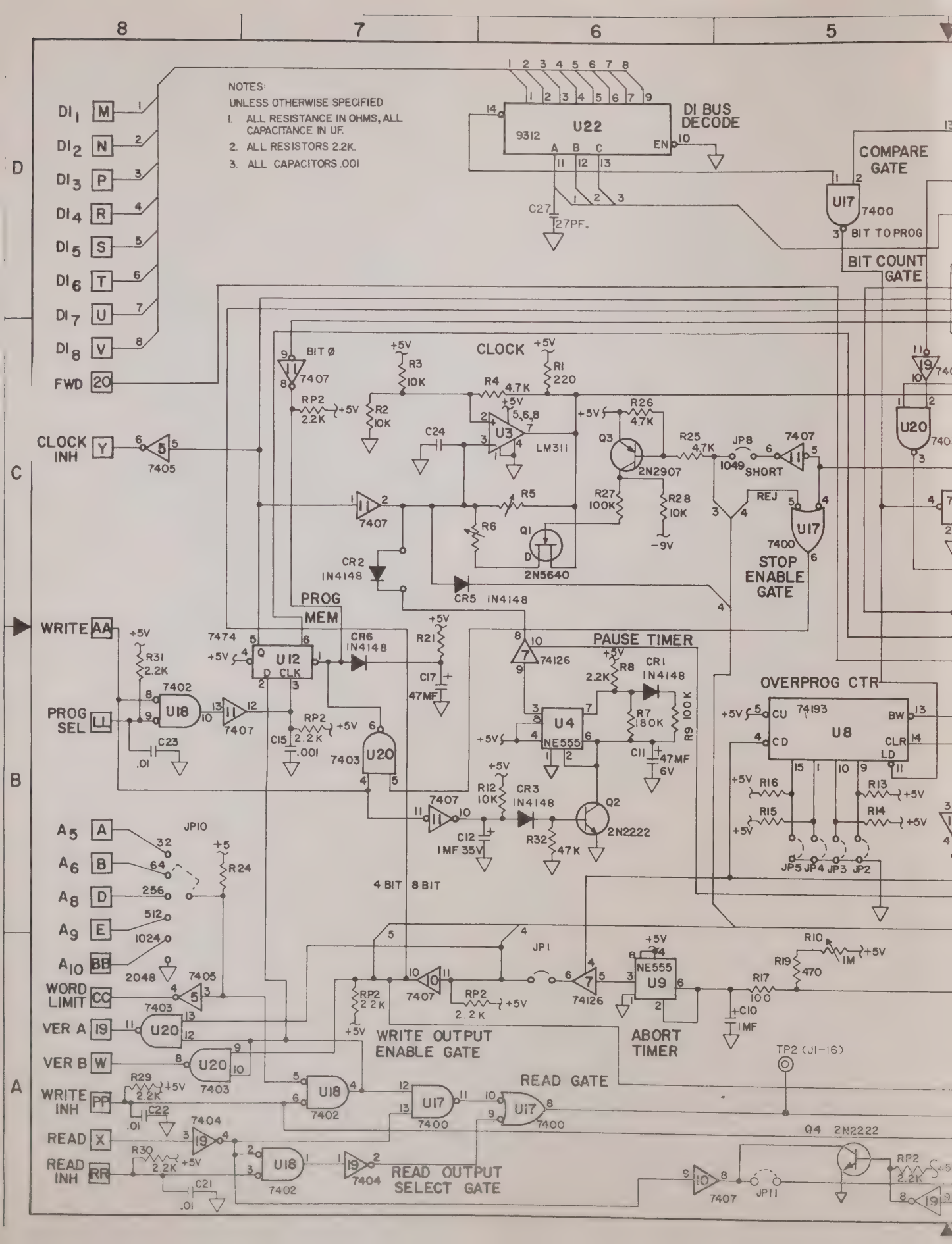
Some dash-numbered card sets are capable of programming both VOL and VOH PROMs by leaving JP6 open and allowing the socket adapter to pull J2-7 low for the VOL parts. For some existing VOL socket adapters, J2-7 is connected to the active high CHIP ENABLE of the PROM being programmed. If this buffer were not present, shorting JP6 to select the VOL mode would disable the PROM. This buffer provides the necessary isolation for Chip Enable in this case.

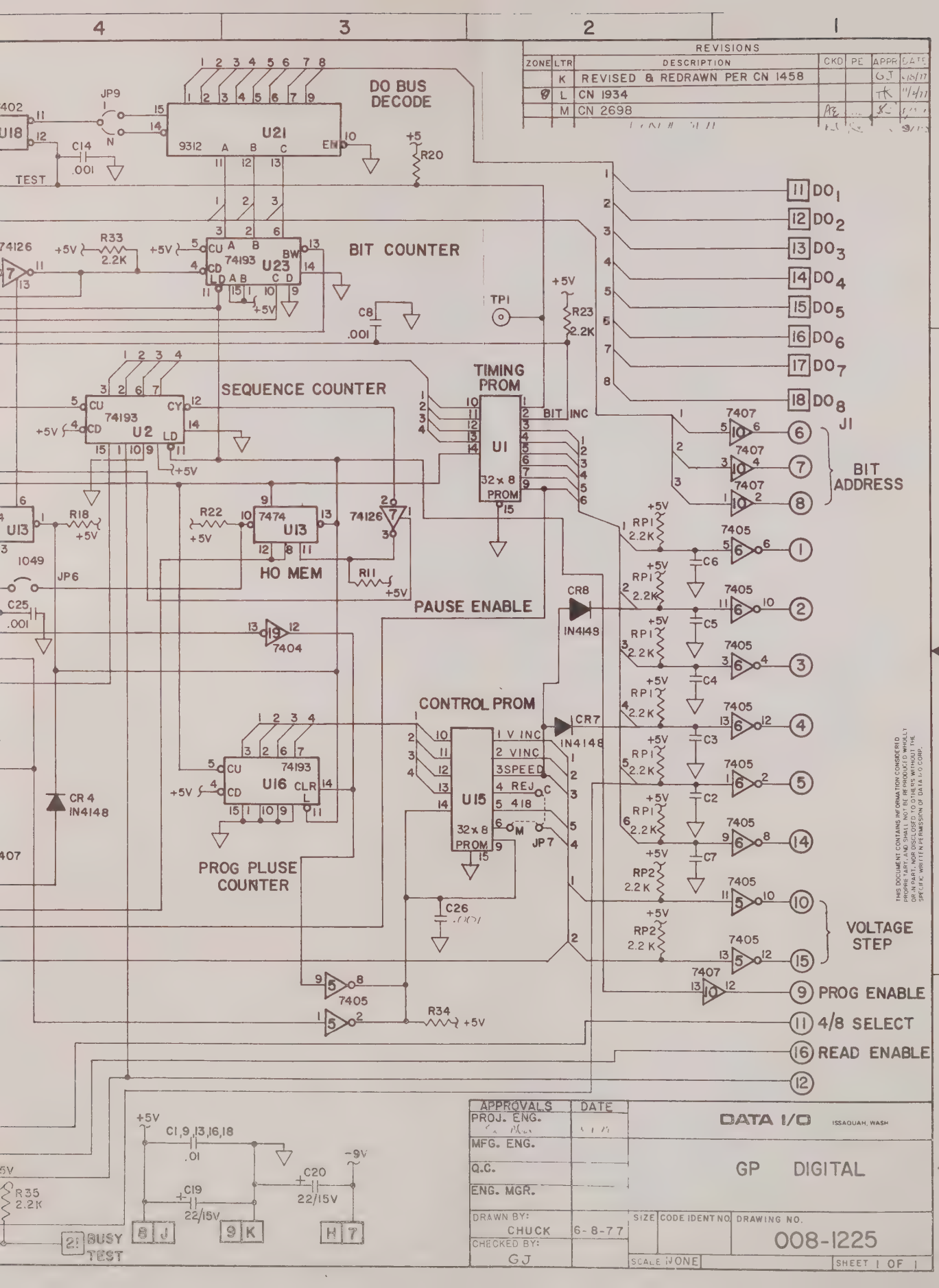
5.3.6 DO BUS DRIVERS

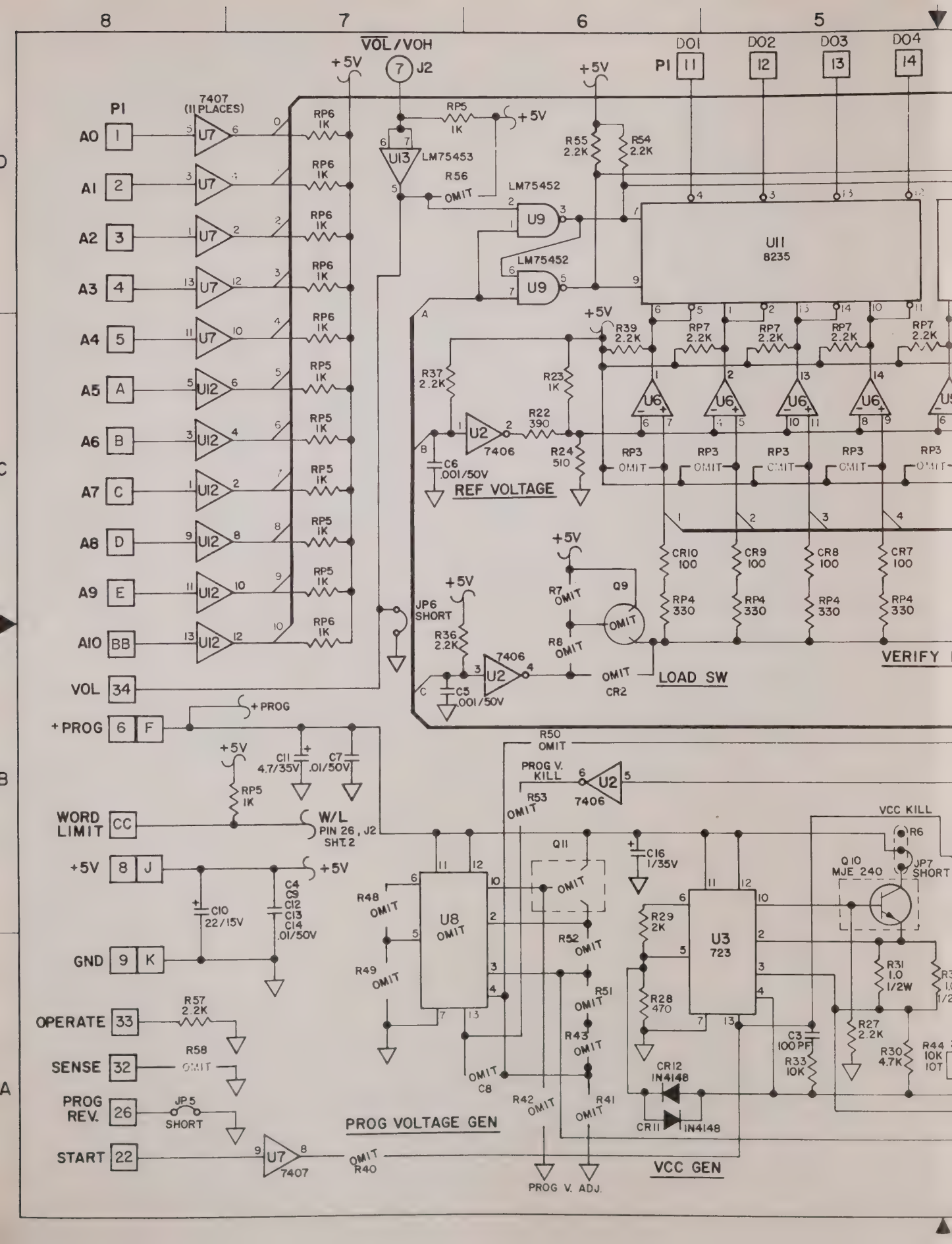
These drivers pass the data from the comparators on to the DO Bus. When VOL is selected, either by shorting JP6 on the analog card or by the socket adapter taking J2-7 low, this data passes through with no inversion. That is, a programmed bit (below threshold on the Comparators) yields a low on the DO Bus. If, however, VOH is selected by JP6 open or by J2-7 high, the data is inverted. In this case a programmed bit (above threshold on the Comparators) is inverted by the bus drivers and again appears as a low on the bus.

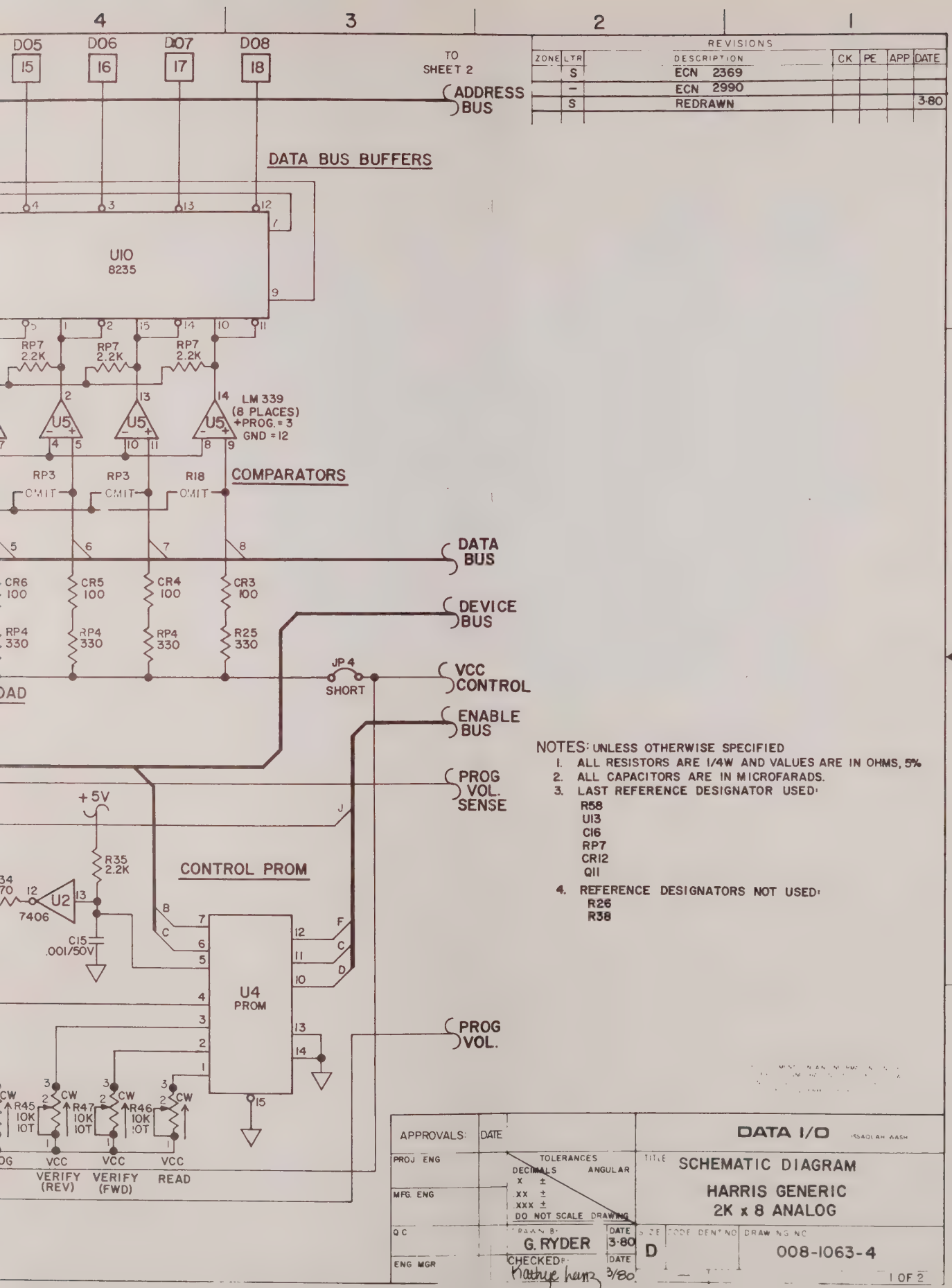
SECTION 6
SCHEMATICS

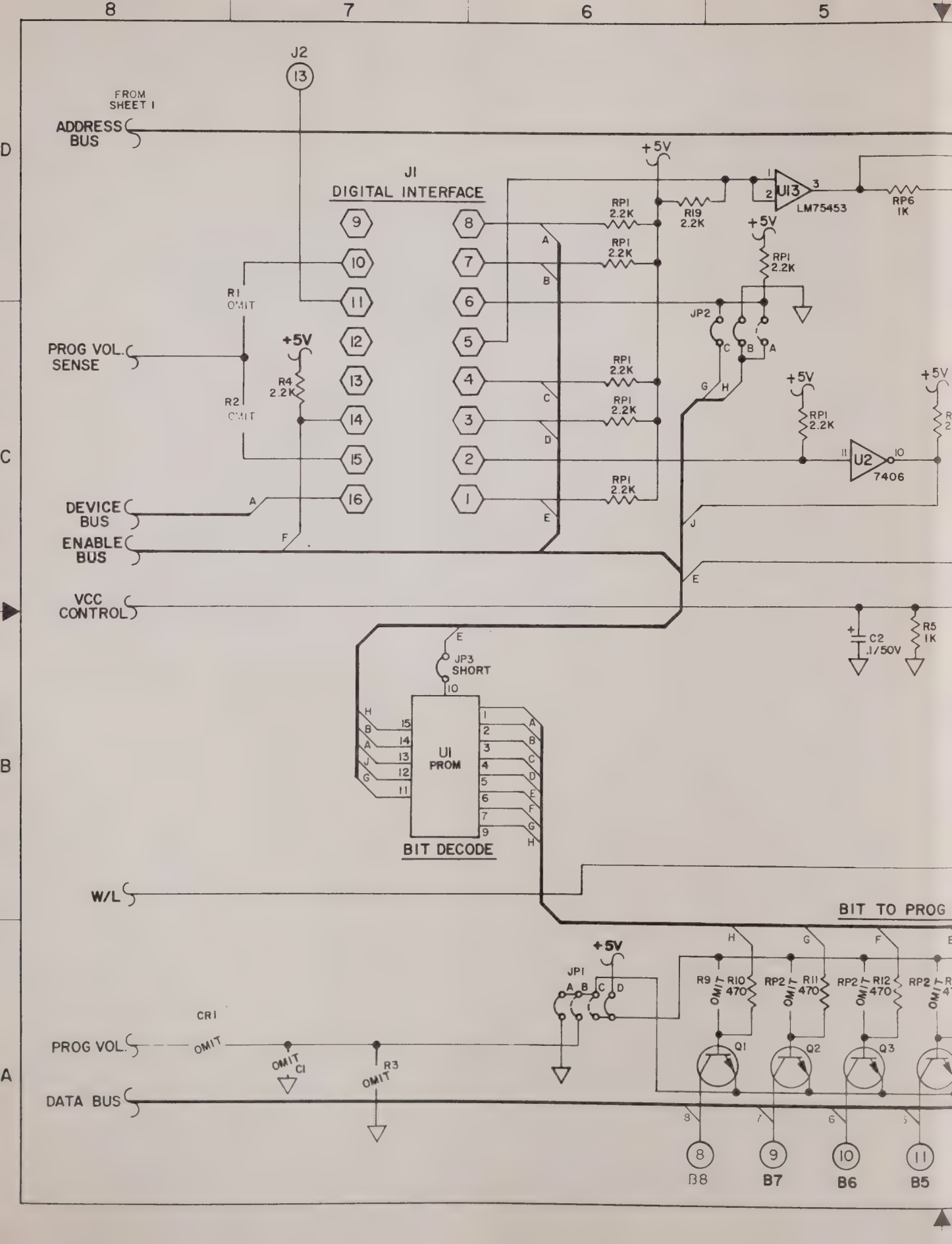
008-1225	GP Digital
008-1063-4	2K x 8 Analog
010-1063-4	Truth Table
008-1072	Plug in Adapter

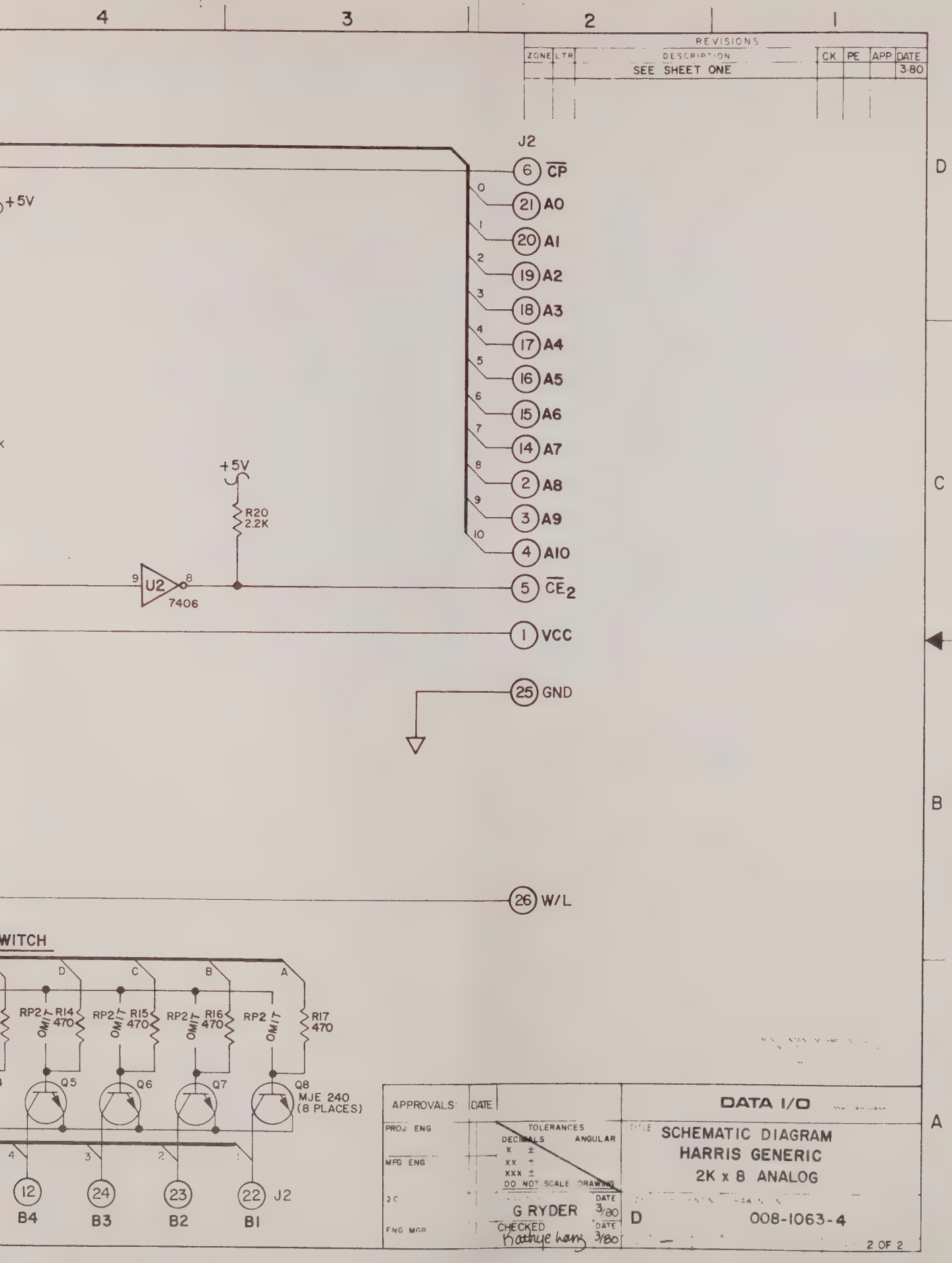

8
7
6
5
D
C
B
A
NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE IN OHMS, ALL CAPACITANCE IN UF.
2. ALL RESISTORS 2.2K.
3. ALL CAPACITORS .001
DI1 M
DI2 N
DI3 P
DI4 R
DI5 S
DI6 T
DI7 U
DI8 V
FWD 20
U22
9312
DI BUS DECODE
C27
27PF.
COMPARE GATE
U17
7400
BIT TO PROG
BIT COUNT GATE
BIT Ø
7407
CLOCK
R3
10K
R1
220
R4
4.7K
RP2
2.2K
R2
10K
U3
LM311
C24
CLOCK INH Y
7405
Q3
2N2907
R26
4.7K
R25
4.7K
JP8
1049
SHORT
R27
100K
R28
10K
-9V
R5
R6
Q1
2N5640
CR2
IN4148
CR5 IN4148
REJ
STOP ENABLE GATE
PROG MEM
WRITE AA
PROG SEL LL
U12
7474
CR6
IN4148
R21
C17
47MF
R31
2.2K
U18
7402
C23
.01
C15
.001
U20
7403
PAUSE TIMER
74126
R8
2.2K
CR1
IN4148
U4
NE555
R7
180K
R9
100K
C11
47MF
6V
OVERPROG CTR
74193
U8
R16
R15
R13
R14
JP5 JP4 JP3 JP2
R12
10K
CR3
IN4148
Q2
2N2222
C12
1MF 35V
R32
47K
A5 A
A6 B
A8 D
A9 E
A10 BB
JP10
32
64
256
512
1024
2048
R24
4 BIT 8 BIT
WORD LIMIT CC
VER A 19
VER B W
JP1
RP2
2.2K
WRITE OUTPUT ENABLE GATE
NE555
U9
ABORT TIMER
R10
1M
R19
470
R17
100
C10
1MF
TP2 (J1-16)
WRITE INH PP
R29
2.2K
C22
.01
READ X
READ INH RR
R30
2.2K
C21
.01
READ GATE
READ OUTPUT SELECT GATE
Q4 2N2222
JP11


REVISIONS
ZONE LTR DESCRIPTION CKD PE APPR DATE
K REVISED & REDRAWN PER CN 1458 GJ 5/5/77
L CN 1934 TK 11/4/77
M CN 2698
DO BUS DECODE
U21
9312
JP9
C14 .001
TEST
+5
R20
BIT COUNTER
U23
74193
R33 2.2K
C8 .001
TP1
R23 2.2K
SEQUENCE COUNTER
U2
TIMING PROM
U1
32 x 8 PROM
BIT INC
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
J1
BIT ADDRESS
7407
7405
RP1 2.2K
RP2 2.2K
C6
C5
C4
C3
C2
C7
R18
R22
R11
U13
7474
7404
HO MEM
JP6
C25 .001
PAUSE ENABLE
CR8 IN4148
CONTROL PROM
U15
32 x 8 PROM
CR7 IN4148
V INC
VINC
SPEED
REJ
418
JP7
C26 .001
CR4 IN4148
U16 CLR
PROG PLUSE COUNTER
VOLTAGE STEP
PROG ENABLE
4/8 SELECT
READ ENABLE
R34
R35 2.2K
BUSY TEST
C1,9,13,16,18 .01
C19 22/15V
C20 22/15V
-9V
THIS DOCUMENT CONTAINS INFORMATION CONSIDERED PROPRIETARY, AND SHALL NOT BE REPRODUCED WHOLLY OR IN PART, NOR DISCLOSED TO OTHERS WITHOUT THE SPECIFIC WRITTEN PERMISSION OF DATA I/O CORP.
APPROVALS DATE
PROJ. ENG.
MFG. ENG.
Q.C.
ENG. MGR.
DRAWN BY: CHUCK 6-8-77
CHECKED BY: GJ
DATA I/O ISSAQUAH, WASH
GP DIGITAL
SIZE CODE IDENT NO DRAWING NO.
008-1225
SCALE NONE
SHEET 1 OF 1


8
7
6
5
VOL/VOH
+5V
J2
P1
DO1
DO2
DO3
DO4
7407 (11 PLACES)
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
VOL
+PROG
WORD LIMIT
W/L PIN 26, J2 SHT 2
GND
OPERATE
SENSE
PROG REV.
START
JP5 SHORT
JP6 SHORT
RP5 1K
RP6 1K
R55 2.2K
R54 2.2K
R56 OMIT
LM75453
LM75452
U11 8235
R39 2.2K
RP7 2.2K
R37 2.2K
R23 1K
R22 390
R24 510
C6 .001/50V
REF VOLTAGE
RP3 OMIT
R36 2.2K
R7 OMIT
R8 OMIT
Q9
CR10 100
CR9 100
CR8 100
CR7 100
RP4 330
LOAD SW
VERIFY
C5 .001/50V
C11 4.7/35V
C7 .01/50V
R50 OMIT
R53 OMIT
PROG V. KILL
R57 2.2K
R58 OMIT
C4 C9 C12 C13 C14 .01/50V
C10 22/15V
U8 OMIT
R48 OMIT
R49 OMIT
R52 OMIT
R51 OMIT
R43 OMIT
R42 OMIT
R41 OMIT
C8 OMIT
Q11 OMIT
C16 1/35V
U3 723
R29 2K
R28 470
R33 10K
C3 100 PF
R27 2.2K
R30 4.7K
R31 1.0 1/2W
Q10 MJE 240
JP7 SHORT
VCC KILL
R6
CR12 IN4148
CR11 IN4148
PROG VOLTAGE GEN
VCC GEN
PROG V. ADJ.
OMIT R40


4
3
2
1
D05
D06
D07
D08
15
16
17
18
TO SHEET 2
ADDRESS BUS
REVISIONS
ZONE LTR DESCRIPTION CK PE APP DATE
S ECN 2369
– ECN 2990
S REDRAWN 3-80
DATA BUS BUFFERS
U10
8235
RP7 2.2K
RP7 2.2K
RP7 2.2K
U5
LM 339
(8 PLACES)
+PROG. = 3
GND = 12
RP3 OMIT
RP3 OMIT
R18 OMIT
COMPARATORS
DATA BUS
CR6 100
CR5 100
CR4 100
CR3 100
RP4 330
RP4 330
RP4 330
R25 330
DEVICE BUS
JP 4
SHORT
VCC CONTROL
ENABLE BUS
PROG VOL. SENSE
+5V
R35 2.2K
CONTROL PROM
U2
7406
C15 .001/50V
U4
PROM
PROG VOL.
R45 10K 10T
R47 10K 10T
R46 10K 10T
CW
VCC VERIFY (REV)
VCC VERIFY (FWD)
VCC READ
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND VALUES ARE IN OHMS, 5%
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED:
R58
U13
C16
RP7
CR12
Q11
4. REFERENCE DESIGNATORS NOT USED:
R26
R38
APPROVALS: DATE
PROJ ENG
MFG. ENG
QC
ENG MGR
TOLERANCES
DECIMALS ANGULAR
X ±
XX ±
XXX ±
DO NOT SCALE DRAWING
DRAWN: G. RYDER DATE 3-80
CHECKED: DATE 3/80
DATA I/O
TITLE SCHEMATIC DIAGRAM
HARRIS GENERIC
2K x 8 ANALOG
SIZE D
CODE IDENT NO
DRAWING NO 008-1063-4
1 OF 2

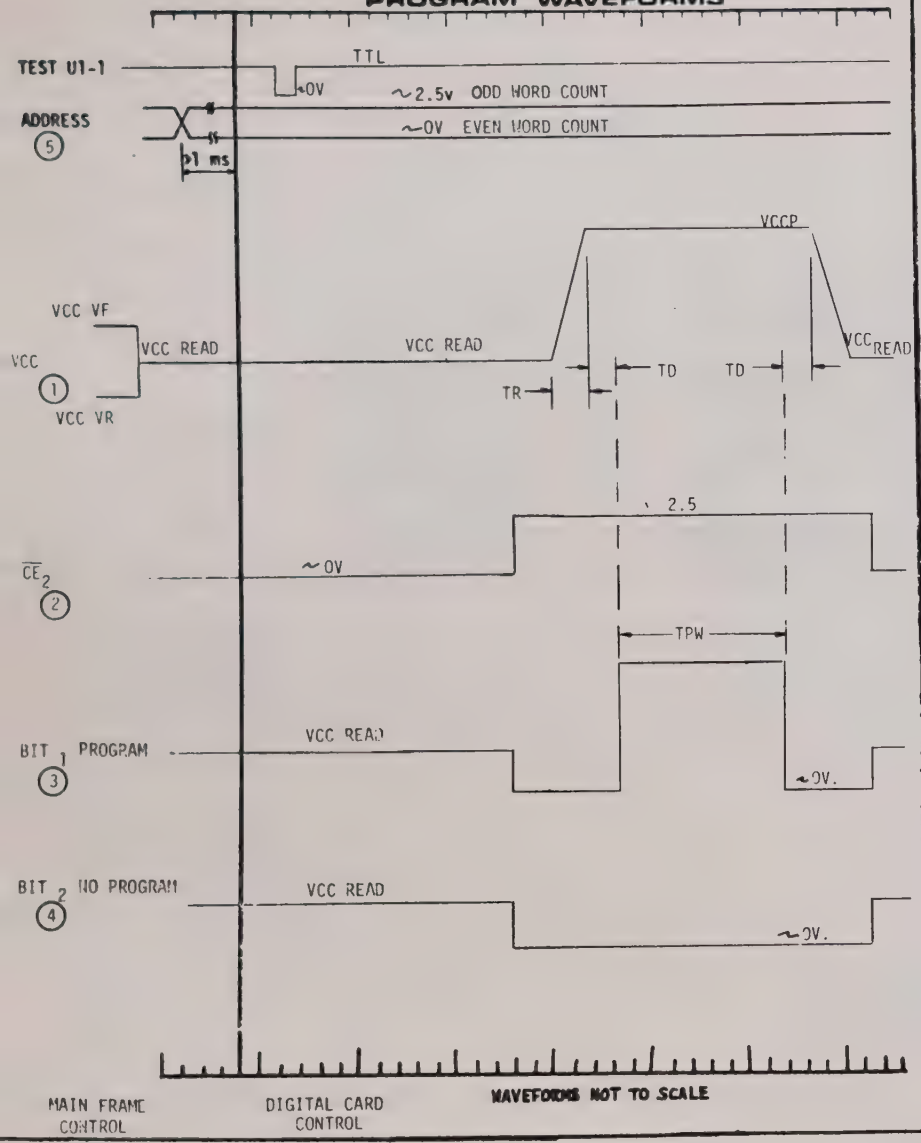

8
7
6
5
D
C
B
A
J2
13
FROM SHEET 1
ADDRESS BUS
J1
DIGITAL INTERFACE
+5V
RP1 2.2K
RI9 2.2K
U13
LM75453
RP6 1K
R1 OMIT
R2 OMIT
R4 2.2K
PROG VOL. SENSE
JP2
U2
7406
DEVICE BUS
ENABLE BUS
VCC CONTROL
C2 .1/50V
R5 1K
JP3 SHORT
U1 PROM
BIT DECODE
W/L
BIT TO PROG
JP1
R9 OMIT
R10 470
R11 470
R12 470
Q1
Q2
Q3
CR1
PROG VOL.
OMIT
C1
R3
DATA BUS
B8
B7
B6
B5


4
3
2
1
REVISIONS
ZONE LTR DESCRIPTION CK PE APP DATE
SEE SHEET ONE 3-80
J2
6 CP
21 A0
20 A1
19 A2
18 A3
17 A4
16 A5
15 A6
14 A7
2 A8
3 A9
4 A10
5 CE2
1 VCC
25 GND
26 W/L
+5V
R20
2.2K
U2
7406
WITCH
RP2 R14 470 OMIT
RP2 R15 470 OMIT
RP2 R16 470 OMIT
RP2 R17 470 OMIT
Q5
Q6
Q7
Q8
MJE 240
(8 PLACES)
12 B4
24 B3
23 B2
22 B1
APPROVALS DATE
PROJ ENG
MFG ENG
QC
ENG MGR
TOLERANCES
DECIMALS ANGULAR
X ±
XX ±
XXX ±
DO NOT SCALE DRAWING
G RYDER 3/80
CHECKED Kathryn Hanz 3/80
DATA I/O
TITLE SCHEMATIC DIAGRAM
HARRIS GENERIC
2K x 8 ANALOG
D 008-1063-4
2 OF 2

2805	ECN# 3431	EF

DATE	SYM	REVISION RECORD	DR
12/7	P	CN# 1997	DS
4/78	R	ECN# 2313	KJ
8/78	S	ECN# 2369	KJ
2-79	-	ECN #2594	FS

PROGRAM WAVEFORMS



NOTES

For calibration, the card set polarity defaults to VOL.

DIGITAL CARD JUMPERS

- JP1 = OPEN
- JP2 = SHORT
- JP3 = SHORT
- JP4 = SHORT
- JP5 = SHORT
- JP6 = SHORT
- JP7C = 8 PULSE REJECT
- JP7M = 1 PULSE REJECT
- JP8 = OPEN
- JP9 = N
- JP10 = WORD LIMIT = 2048
- JP11 = OPEN

ABORT TIMER = JP1 = NOT USED

PAUSE TIMER (CR2) = NOT USED

WAVEFORM VARIABLES

PROGRAMMING DUTY CYCLE 34%

TD ≥ 10 μ sec.

TPW = 100 + 10 μ sec.

TR = 2-10uS
VCC VR = 4.5 ± .2 volts
VCC READ = 5.0 ± .2 volts

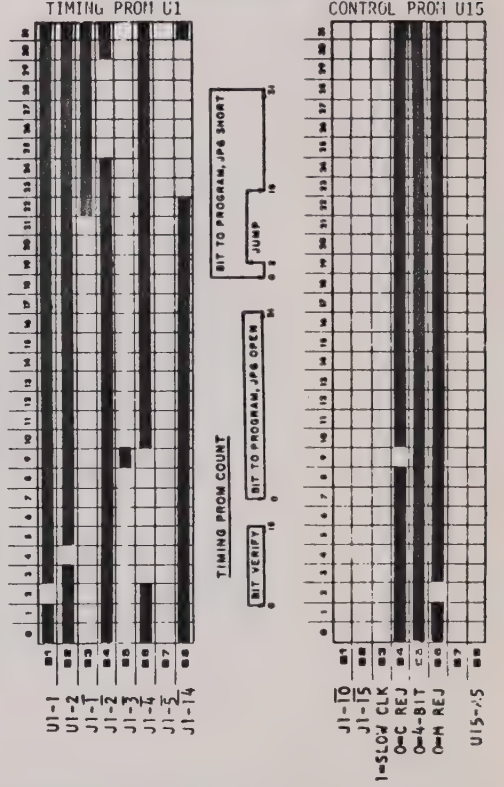
VCC VF = 5.5 ± .2 volts

VCCP = VOP = 12.25 ± .25 volts

(1) THESE WAVEFORMS CORRESPOND TO CALLOUTS ON THE CALIBRATION CHART. SWITCH S2 AND S3 OF THE UNIVERSAL CALIBRATOR TO INDICATED POSITIONS TO OBTAIN WAVEFORMS. REFER TO PERFORMANCE CHECK SECTION OF MANUAL FOR DETAILED STEPS.

TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)



DATA I/O ISSAQUAH WASH.

TIMING DIAGRAM

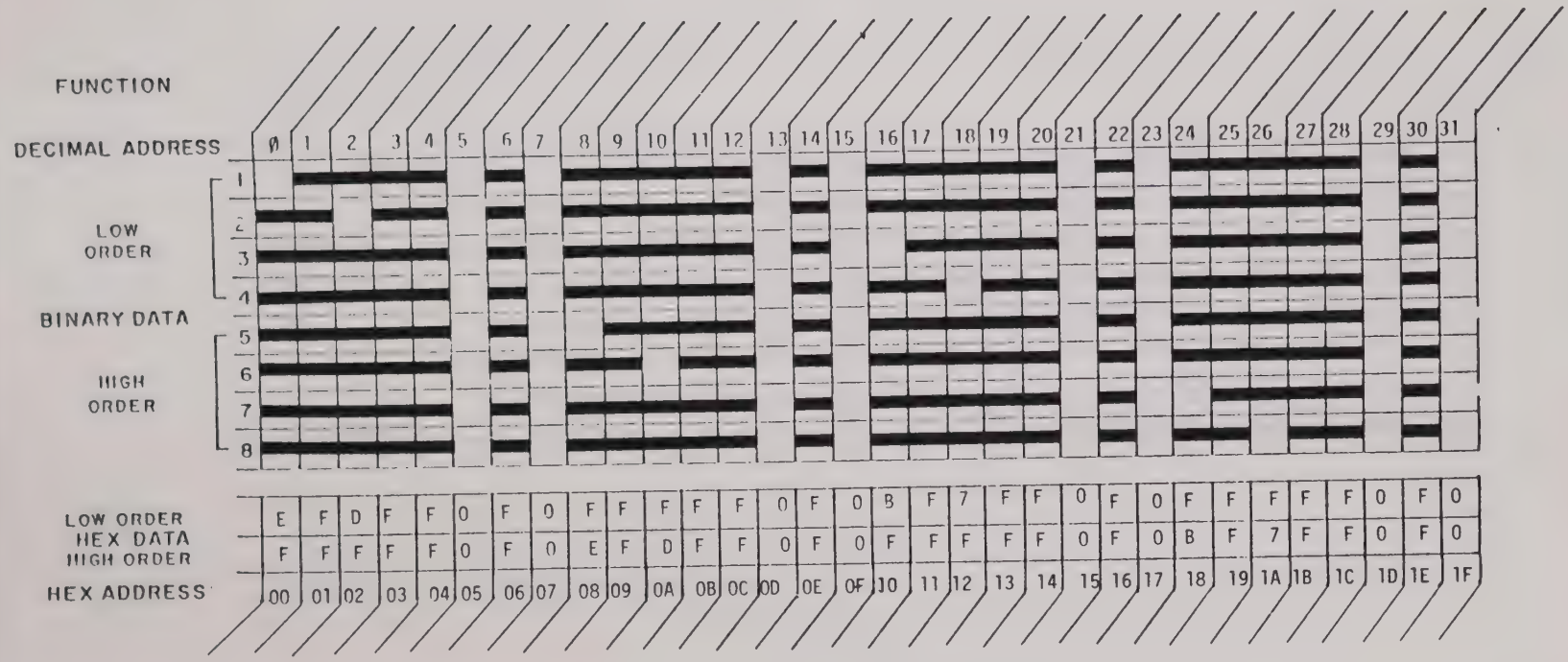
K.J.

G.T.

HARRIS GENERIC

9-2-76 | 007-1063-4

DATE	BY	REVISION RECORD	DR	CK
12-7-77	P	C.N. #1997	PW	
6-23-78	R	ECN #2313	KJ	
8-7-78	S	ECN #2369	KJ	RO
10-29-79-		ECN #3277		


FUNCTION
DECIMAL ADDRESS
Ø 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
LOW ORDER
BINARY DATA
HIGH ORDER
1
2
3
4
5
6
7
8
LOW ORDER HEX DATA HIGH ORDER
E F D F F 0 F 0 F F F F F 0 F 0 B F 7 F F 0 F 0 F F F F F 0 F 0
F F F F F 0 F 0 E F D F F 0 F 0 F F F F F 0 F 0 B F 7 F F 0 F 0
HEX ADDRESS
00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F

NOTES

LINE = HIGH

NO LINE = LOW

PROM LABEL

1A-1063-4S

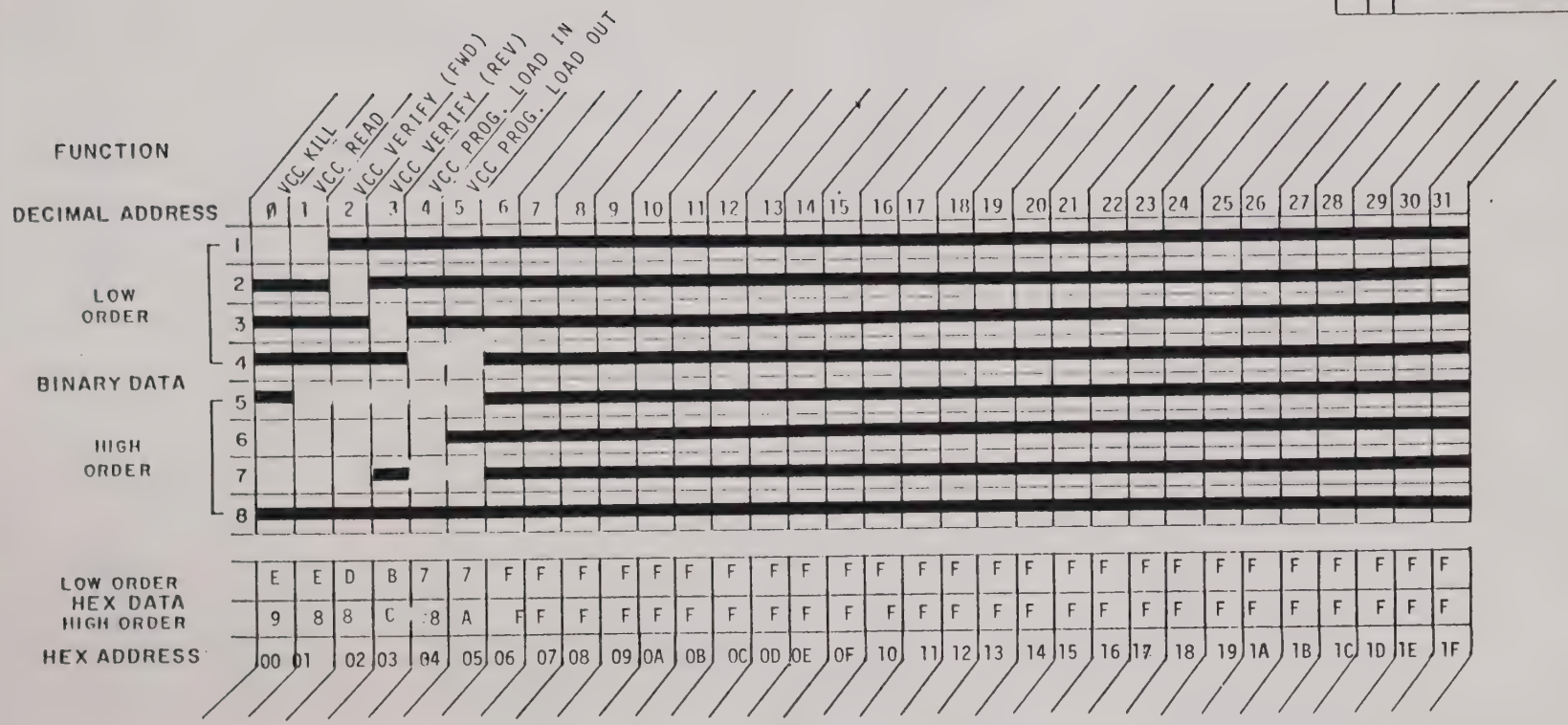
"U" LOCATION

CARD NUMBER

DASH AND REVISION

TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL . —	HARRIS GENERIC	SCALE --	DRAWN BY P. WALTER
FRACTIONAL . —	TITLE 2Kx8 ANALOG		APPROVED BY
ANGULAR . —	DATE 12-7-77	DRAWING NUMBER 010-1063-4	SHT 1/2

DATE	BY	REVISION RECORD	DR	CK
		See Sheet 1/2 ● 2		


FUNCTION
DECIMAL ADDRESS
0 VCC KILL
1 VCC READ
2 VCC VERIFY (FWD)
3 VCC VERIFY (REV)
4 VCC PROG. LOAD IN
5 VCC PROG. LOAD OUT
6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
LOW ORDER
BINARY DATA
HIGH ORDER
1 2 3 4 5 6 7 8
LOW ORDER HEX DATA
HIGH ORDER
HEX ADDRESS
E E D B 7 7 F F F F F F F F F F F F F F F F F F F F F F F F F F
9 8 8 C 8 A F F F F F F F F F F F F F F F F F F F F F F F F F F
00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F

PROM LABEL

4A-1063-4S

"U" LOCATION

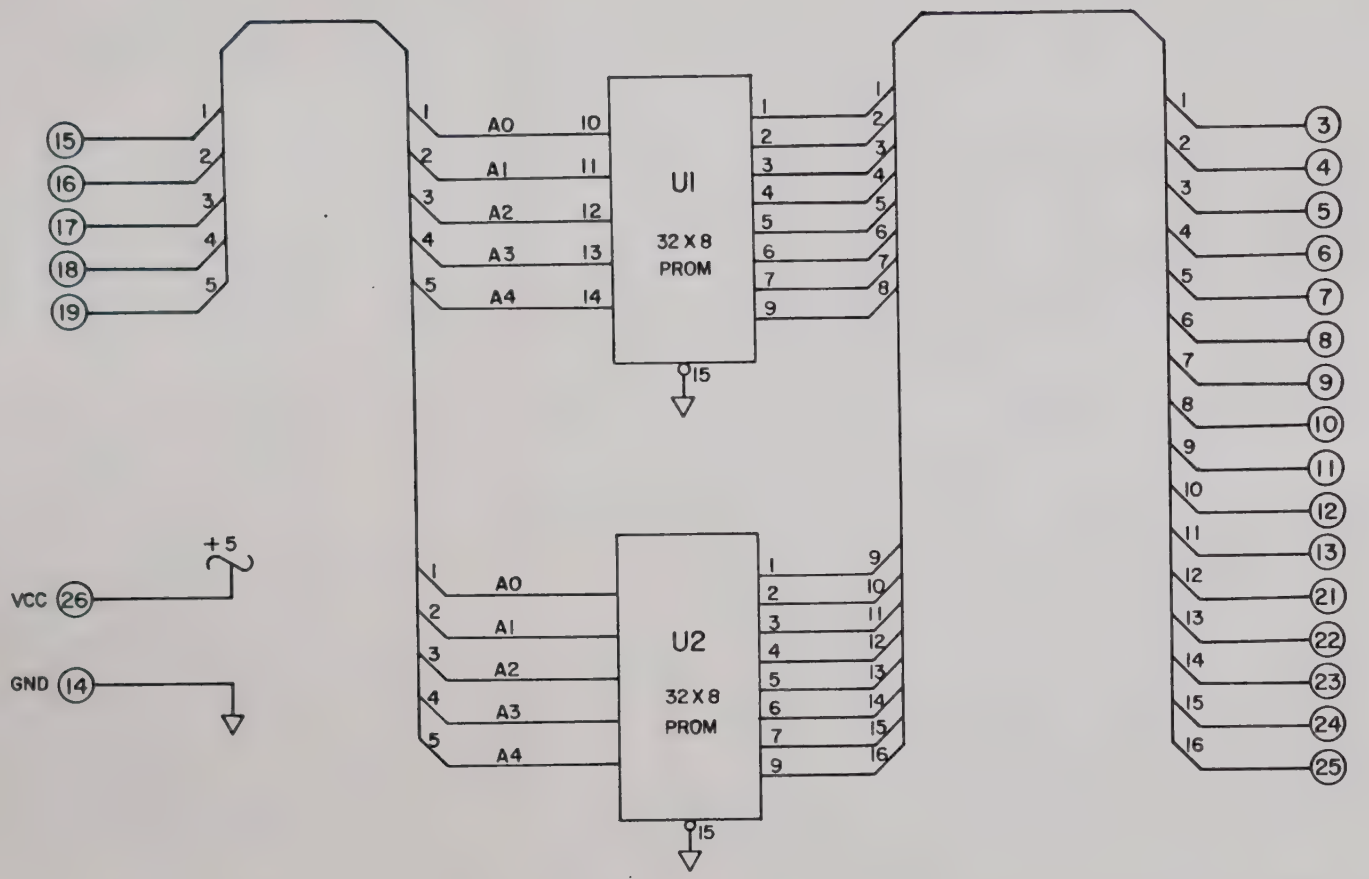
CARD NUMBER

DASH AND REVISION

TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL . —	HARRIS GENERIC	SCALE --	DRAWN BY P.WALTER
FRACTIONAL . —	TITLE 2Kx8 ANALOG		APPROVED BY
ANGULAR . —	DATE 12-7-77	DRAWING NUMBER 010-1063-4	SHT 2/2

2/2

DATE	SYM	REVISION RECORD	DR	CK
11-15 75	A	RELEASE		



TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL ±		SCALE	DRAWN BY G. ROPPE
FRACTIONAL ±	TITLE PLUG IN ADAPTER (UNIVERSAL CALIBRATOR)		APPROVED BY
ANGULAR ±	DATE 10-15-75	DRAWING NUMBER 008-1072	

DATA I/O

Programming systems for tomorrow...today

Reader Comments

The manual's completeness, accuracy, organization, usability, and reliability: _____

_____

Did you find errors in this manual: _____

How can this manual be improved: _____

_____

_____

Additional comments: _____

_____

Name _____

Company _____ Department _____ M/S _____

Address _____

City _____ State _____ Zip _____ Phone _____

Manual or Part No. _____

Warranty/Registration

Please return this card to Data I/O within five days

Did the packaging of this equipment exhibit any outward signs of physical damage? . . . . . YES ○ ○ NO
Did this equipment arrive intact, without loose parts or cable damage? . . . . . YES ○ ○ NO
Did the equipment operate on power-up?. . . . . YES ○ ○ NO
Did you attain adequate system performance? . . . . . YES ○ ○ NO
Were any electrical adjustments required? . . . . . YES ○ ○ NO
If you required assistance, was a local Data I/O representative contacted? . . . . . YES ○ ○ NO

Comments – _____

_____

Name _____ Title _____

Department _____ M/S _____

Company _____

Address _____

City _____ State _____ Zip _____ Phone ( ) _____

Model or Description _____ Serial or Part No. _____

Date Received _____

90 Day Warranty

Data I/O warrants that all equipment sold pursuant to any resultant agreement shall be free from defects in material or workmanship at the time of delivery. Such warranty shall extend for 90 days. Buyer must provide notice to Data I/O within this prescribed warranty period of any defect; if the defect is not the result of improper usage, service, maintenance or installation and equipment has not been otherwise damaged or modified after delivery, Data I/O shall either replace or repair the defective part or parts of equipment or replace the equipment or refund the purchase price at Data I/O's option after return of such equipment by buyer to Data I/O. Shipment to and from Data I/O's facility shall be borne on account of buyer.

(a) Consequential Damages — Data I/O shall not be liable for any incidental or consequential damages incurred as a result of any defect in any equipment sold hereunder and Data I/O's liability is specifically limited to its obligation described herein to repair or replace a defective part or parts covered by this warranty.

(b) Exclusive Warranty — The warranty set forth herein is the only warranty, oral or written made by Data I/O and is in lieu of and replaces all other warranties, expressed or implied, including the WARRANTY OF MERCANTIBILITY AND THE WARRANTY OF FITNESS FOR PARTICULAR PURPOSE.

DATA I/O
Programming systems for tomorrow...today

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL FIRST CLASS Permit No. 24 Issaquah, WA 98027

Postage will be paid by:

DATA I/O Reader Comments

Director of Sales Support
P. O. Box 308
1297 Northwest Mall
Issaquah, WA 98027

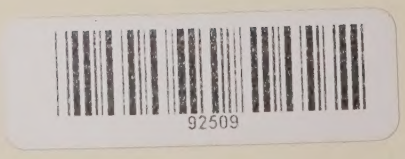
NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL FIRST CLASS Permit No. 24 Issaquah, WA 98027

Postage will be paid by:

DATA I/O Warranty/Registration

Service Manager
P. O. Box 308
1297 Northwest Mall
Issaquah, WA 98027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